EC200A Series

Hardware Design

LTE Standard Module Series

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The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergent help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2022-01-05	Anthony LIU/ Kexiang ZHANG	Creation of the document
1.0	2022-01-11	Anthony LIU/ Kexiang ZHANG	First official release
1.1	2022-12-01	Stephen HE/ Kexiang ZHANG	1. Added the applicable module EC200A-EL and related information. 2. Updated the information about USB serial drivers (Chapter 2.2). 3. Opened WLAN interface (Figures 1, 2, Tables 4, 6 and Chapter 4.13). 4. Updated the pin 3 from RESERVED to SLEEP_IND and added related description (Figure 2, Tables 6 and 24). 5. Added the DC characteristics of the pins in RGMII/RMII interface (Table 6). 6. Updated the comment of RGMII/RMII_RST_N pins (Tables 6 and 23). 7. Updated the VBAT_RF current capability requirement from 1.8 A to 2.0 A (Tables 6, 8 and 39). 8. Added the USIM_GND pin and related description (Tables 6 and 13). 9. Updated the conditions for enabling the module into sleep mode in the UART application scenario (Chapter 3.2.1). 10. Updated current requirements for power supply capabilities (Chapter 3.4.2). 11. Updated the time difference between powering up VBAT and pulling down PWRKEY

	(Chapter 3.5). 12. Updated the turn-off timing diagram and added related information (Chapter 3.6.1). 13. Updated the data of power consumption (Chapter 6.3). 14. Updated the data of digital I/O characteristic (Chapter 6.4). 15. Updated the recommended thermal profile parameters (Figure 45 and Table 52).

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1 Introduction

This document defines the EC200A series module and describes its air interfaces and hardware interfaces which are connected with customers' applications.

It can help customers quickly understand interface specifications, electrical and mechanical details, as well as other related information of the module. Associated with application notes and user guides, customers can use this module to design and to set up mobile applications easily.

1.1. Special Marks

Table 1: Special Marks

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of such model is currently unavailable.
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SD_SDIO_DATA[0:3] refers to all four SD_SDIO_DATA pins, SD_SDIO_DATA0, SD_SDIO_DATA1, SD_SDIO_DATA2, and SD_SDIO_DATA3.

2 Product Overview

EC200A is a series of LTE-FDD/LTE-TDD/WCDMA/GSM wireless communication module with receive diversity, which provides data connectivity on LTE-FDD, LTE-TDD, HSDPA, HSUPA, HSPA+, WCDMA, EDGE and GPRS network data connection. It also provides voice functionality for your specific applications. EC200A series contains four variants: EC200A-CN, EC200A-AU, EC200A-EU and EC200A-EL. You can choose a dedicated type based on the region or operator. The following table shows the frequency bands of EC200A series module.

Table 2: Brief Introduction of the Module

Categories	
Packaging and pins number	LCC 80-pin; LGA 64-pin
Dimensions	(29.0 ±0.15) mm × (32.0 ±0.15) mm × (2.4 ±0.2) mm
Weight	4.4 g
Wireless network functions	LTE/WCDMA/GSM
Variants	EC200A-CN, EC200A-AU, EC200A-EU, EC200A-EL

2.1. Frequency Bands and Functions

Table 3: Wireless Network Type

Wireless Network Types	EC200A-CN	EC200A-AU	EC200A-EU	EC200A-EL
LTE-FDD	B1/B3/B5/B8	B1/B2/B3/B4/B5/B7/B8/B28/B66	B1/B3/B5/B7/B8/B20/B28	B1/B3/B5/B7/B8/B20/B28
LTE-TDD	B34/B38/B39/B40/B41	B40	B38/B40/B41	B38/B40/B41
WCDMA	B1/B5/B8	B1/B2/B4/B5/B8	B1/B5/B8	B1/B5/B8
GSM	900/1800 MHz	850/900/1800/1900 MHz	900/1800 MHz	-

2.2. Key Features

Table 4: Key Features

Features	Details
Power Supply	● Supply voltage: 3.4–4.5 V ● Typical supply voltage: 3.8 V
SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
(U)SIM Interface	● Supports (U)SIM card: 1.8/3.0 V
Audio Features	● Supports one digital audio interface: PCM Interface ● Supports one analog audio interface: MIC/SPK Interface ● GSM: HR/FR/EFR/AMR/AMR-WB ● WCDMA: AMR/AMR-WB ● LTE: AMR/AMR-WB ● Supports echo cancellation and noise suppression.
PCM Interface	● Used for audio function with external codec ● Supports 16 format ● Supports short frame ● Supports master and slave modes*
Analog audio Interface	● Supports one analog audio input and one analog audio output channel
SPI Interface	● Supports one SPI interface ● Maximum clock frequency 52 MHz ● Supports master mode
I2C Interface	● Supports one I2C interface ● Complies with I2C bus protocol specifications (100/400 kHz) ● The multi-host mode is not supported
USB Interface	● Compliant with USB 2.0 specification (slave only); the data transfer rate can reach up to 480 Mbps ● Used for AT command communication, data transmission, software debugging and firmware upgrade ● Supports USB serial driver for Windows 7/8/8.1/10/11, Linux 2.6–5.18 and Android 4.x–12.x systems
WLAN Interface	● Supports SDIO interface for WLAN function
SD Interface	● Supports SD 3.0 protocol.

RGMII*/RMII Interface	● Supports RMII: 1.8/3.3 V ● Supports RGMII: 1.8 V
UART Interfaces	**Main UART:** ● Used for AT command communication and data transmission ● Baud rate: 115200 bps by default, Max. 921600 bps ● Supports RTS and CTS hardware flow control **Debug UART:** ● Used for the output of partial logs ● Baud rate: 115200 bps.
ADC Interfaces	● Supports two ADC interfaces ● Voltage range: 0 V–VBAT_BB
Network Indication	● NET_MODE and NET_STATUS to indicate network connectivity status
AT Commands	● Compliant with *3GPP TS 27.007*, *3GPP TS 27.005* and Quectel enhanced AT commands
Rx-diversity	● Supports LTE Rx-diversity
Antenna Interface	● Main antenna interface (ANT_MAIN) and Rx-diversity antenna interface (ANT_DRX) ● 50 Ω impedance
Transmitting Power	● GSM850: Class 4 (33 dBm ±2 dB) ● EGSM900: Class 4 (33 dBm ±2 dB) ● DCS1800: Class 1 (30 dBm ±2 dB) ● PCS1900: Class 1 (30 dBm ±2 dB) ● GSM850 8-PSK: Class E2 (27 dBm ±3 dB) ● EGSM900 8-PSK: Class E2 (27 dBm ±3 dB) ● DCS1800 8-PSK: Class E2 (26 dBm ±3 dB) ● PCS1900 8-PSK: Class E2 (26 dBm ±3 dB) ● WCDMA: Class 3 (24 dBm +1/-3 dB) ● LTE-FDD: Class 3 (23 dBm ±2 dB) ● LTE-TDD: Class 3 (23 dBm ±2 dB)
LTE Features	● Supports 3GPP R9 non-CA Cat 4 FDD and TDD ● Supports 1.4/3/5/10/15 to 20 MHz RF bandwidth ● Supports MIMO in DL direction ● Supports uplink QPSK, 16-QAM modulation ● Supports downlink QPSK, 16-QAM and 64-QAM modulation ● FDD: Max. 150 Mbps (DL)/ 50 Mbps (UL) ● TDD: Max. 130 Mbps (DL)/ 30 Mbps (UL)
UMTS Features	● Supports 3GPP R7 HSPA+/HSDPA/HSUPA and WCDMA ● Supports QPSK, 16QAM, 64QAM modulation ● HSPA+: Max. 21 Mbps (DL) ● HSUPA: Max. 5.76 Mbps (UL) ● WCDMA: Max. 384 kbps (DL)/384 kbps (UL)
GSM Features	**GPRS:**

	● Supports GPRS multi-slot class 12 ● Coding scheme: CS 1–4 ● Max. 85.6 kbps (DL)/85.6 kbps (UL) **EDGE:** ● Supports EDGE multi-slot class 12 ● Supports GMSK and 8–PSK for different MCS (Modulation and Coding Scheme) ● Downlink coding schemes: MCS 1–9 ● Uplink coding schemes: MCS 1–9 ● Max. 236.8 kbps (DL)/236.8 kbps (UL)
Internet Protocol Features	● Supports TCP/UDP/PPP/NTP/NITZ/FTP/HTTP/PING/CMUX/ HTTPS/FTPS/SSL/FILE/MQTT/MMS/SMTP/SMTPS protocols ● Supports PAP and CHAP for PPP connections
Temperature Range	● Operating temperature range [1]: -35 to +75 °C ● Extended temperature range [2]: -40 to +85 °C ● Storage temperature range: -40 to +90 °C
Firmware Upgrade	Use USB interface or DFOTA to upgrade.
RoHS	All hardware components are fully compliant with EU RoHS directive.

[1] Within the operating temperature range, the module meets 3GPP specifications.
[2] Within the extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as Pout, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

2.3. Functional Diagram

The following figure shows a block diagram of the module and illustrates the major functional parts.

- Power management
- Baseband
- DDR + NAND flash
- Radio frequency
- Peripheral interface

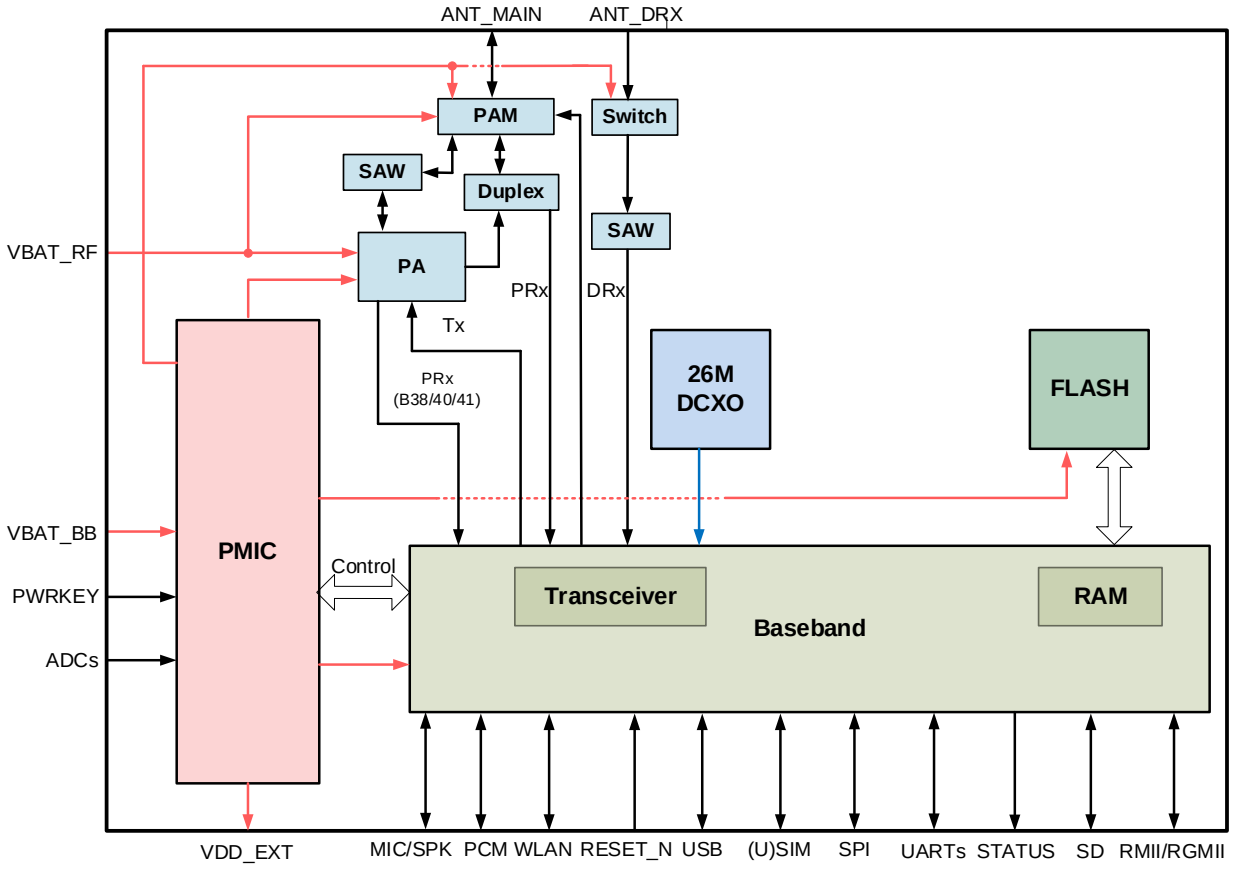


Figure 1: Functional Diagram

2.4. Pin Assignment

The following figure illustrates the pin assignment of the module.

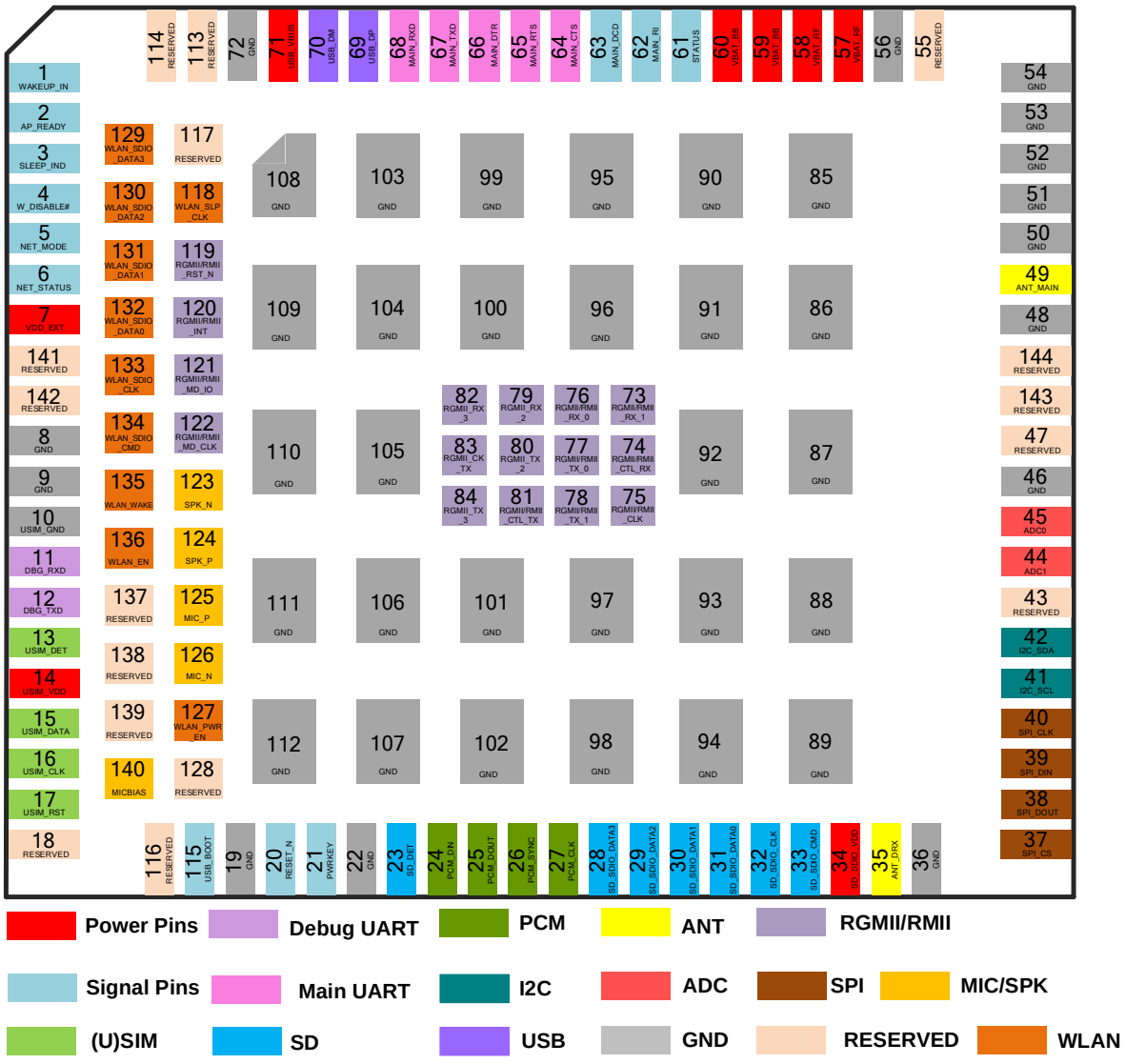


Figure 2: Pin Assignment (Top View)

NOTE

1. The USB_BOOT and RGMII/RMII_RST_N pins cannot be pulled up to high level before the module is powered on successfully.
2. Unused and RESERVED pins are kept open and all GND pins are connected to the ground network.

2.5. Pin Description

The following table shows the DC characteristics and pin descriptions.

Table 5: I/O Parameters Definition

Type	Description
AI	Analog Input
AIO	Analog Input/Output
AO	Analog Output
DI	Digital Input
DIO	Digital Input/Output
DO	Digital Output
OD	Open Drain
PI	Power Input
PO	Power Output

Table 6: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	59, 60	PI	Power supply for the module's baseband part	Vmax = 4.5 V Vmin = 3.4 V Vnom = 3.8 V	It must be provided with sufficient current up to 0.8 A.
VBAT_RF	57, 58	PI	Power supply for the module's RF part	Vmax = 4.5 V Vmin = 3.4 V Vnom = 3.8 V	It must be provided with sufficient current up to 2.0 A.
VDD_EXT	7	PO	Provide 1.8 V for external circuit	Vmin = 1.67 V Vnom = 1.8 V Vmax = 1.93V $I_O$max = 50 mA	It can provide a pull-up power to the external GPIO. If unused, keep it open.
GND	8, 9, 19, 22, 36, 46, 48, 50–54, 56, 72, 85–112				

Turn On/Off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	21	DI	Turn on/off the module	V_{IL}max = 0.5 V	VBAT power domain. Active low.
RESET_N	20	DI	Reset the module		1.8 V power domain. Active low after turn-on.
Indication Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	61	OD	Indicate the module's operation status	VDD_EXT	1.8 V power domain. If unused, keep them open.
NET_STATUS	6	DO	Indicate the module's network activity status		
NET_MODE	5	DO	Indicate the module's network registration mode		
SLEEP_IND	3	DO	Indicate the module's sleep mode		
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	71	AI	USB connection detect	Vmax = 5.25 V Vmin = 3.0 V Vnom = 5.0 V	Typ. 5.0 V. If unused, keep it open.
USB_DP	69	AIO	USB differential data (+)		90 Ω differential impedance. USB 2.0 compliant. If unused, keep them open.
USB_DM	70	AIO	USB differential data (-)		
(U)SIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_VDD	14	PO	(U)SIM card power supply	**Low-voltage:** Vmin = 1.67 V Vnom = 1.8 V Vmax = 1.93 V	Either 1.8 V or 3.0 V (U)SIM card is supported and

				High-voltage: Vmin = 2.7 V Vnom = 3.0 V Vmax = 3.3 V	can be identified automatically by the module.
USIM_DATA	15	DIO	(U)SIM card data	USIM_VDD	
USIM_CLK	16	DO	(U)SIM card clock		
USIM_RST	17	DO	(U)SIM card reset		
USIM_DET	13	DI	(U)SIM card hot-plug detect	VDD_EXT	1.8 V power domain. If unused, keep it open.
USIM_GND	10		Dedicated ground for (U)SIM card		Connect to the ground of (U)SIM card.
SD Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SD_SDIO_CLK	32	DO	SD card SDIO clock	SD_SDIO_VDD	1.8/2.8 V power domain. If unused, keep them open.
SD_SDIO_CMD	33	DIO	SD card SDIO command		
SD_SDIO_DATA0	31	DIO	SD card SDIO bit 0		
SD_SDIO_DATA1	30	DIO	SD card SDIO bit 1		
SD_SDIO_DATA2	29	DIO	SD card SDIO bit 2		
SD_SDIO_DATA3	28	DIO	SD card SDIO bit 3		
SD_SDIO_VDD	34	PO	SD card SDIO power supply	**Low-voltage:** Vmin = 1.67 V Vnom = 1.8 V Vmax = 1.93 V **High-voltage:** Vmin = 2.7 V Vnom = 2.8 V Vmax = 3.05 V	
SD_DET*	23	DI	SD card hot-plug detect	VDD_EXT	1.8 V power domain. If unused, keep it open.

Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_RI	62	DO	Main UART ring indication	VDD_EXT	1.8 V power domain. If unused, keep them open.
MAIN_DCD	63	DO	Main UART data carrier detect		
MAIN_CTS	64	DO	DTE clear to send signal from DCE (Connect to DTE's CTS)		
MAIN_RTS	65	DI	DTE request to send signal to DCE (Connect to DTE's RTS)		
MAIN_DTR	66	DI	Main UART data terminal ready		
MAIN_RXD	68	DI	Main UART receive		
MAIN_TXD	67	DO	Main UART transmit		
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	11	DI	Debug UART receive	VDD_EXT	1.8 V power domain. If unused, keep them open.
DBG_TXD	12	DO	Debug UART transmit		
SPI Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI_CS	37	DO	SPI chip select	VDD_EXT	1.8 V power domain. If unused, keep them open.
SPI_DOUT	38	DO	SPI data output		
SPI_DIN	39	DI	SPI data input		
SPI_CLK	40	DO	SPI clock		
I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SCL	41	OD	I2C serial clock		Used for external codec. An external
I2C_SDA	42	OD	I2C serial data		

					1.8 V pull-up resistor is needed.
PCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_SYNC	26	DIO	PCM data frame sync	VDD_EXT	1.8 V power domain. When the module is the master device, this pin is in the output state while when the module is used as a slave* device, it is in the input state. If unused, keep them open.
PCM_CLK	27	DIO	PCM clock		
PCM_DIN	24	DI	PCM data input		1.8 V power domain. If unused, keep them open.
PCM_DOUT	25	DO	PCM data output		
WLAN Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WLAN_SLP_CLK*	118	DO	WLAN sleep clock	VDD_EXT	1.8 V power domain. If unused, keep them open.
WLAN_PWR_EN	127	DO	WLAN power supply enable control		
WLAN_SDIO_DATA3	129	DIO	WLAN SDIO data bit 3		
WLAN_SDIO_DATA2	130	DIO	WLAN SDIO data bit 2		
WLAN_SDIO_DATA1	131	DIO	WLAN SDIO data bit 1		
WLAN_SDIO_DATA0	132	DIO	WLAN SDIO data bit 0		
WLAN_SDIO_CLK	133	DO	WLAN SDIO clock		
WLAN_SDIO_CMD	134	DO	WLAN SDIO command		
WLAN_WAKE	135	DI	Wake up the host by an external Wi-Fi module		

WLAN_EN	136	DO	WLAN function enable control		
RF Antenna Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_DRX	35	AI	Diversity antenna interface		50 Ω impedance.
ANT_MAIN	49	AIO	Main antenna interface		
ADC Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	45	AI	General-purpose ADC interface	Voltage Range: 0 V–VBAT_BB	If unused, keep them open.
ADC1	44	AI			
RGMII*/RMII Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RGMII/RMII_RX_1	73	DI	RGMII/RMII receive data bit 1	**1.8V RGMII/RMII:** V_{IL}min = -0.3 V V_{IL}max = 0.54 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V V_{OL}max = 0.2 V V_{OH}min = 1.6 V **3.3 V RMII:** V_{IL}min = -0.3 V V_{IL}max = 0.8 V V_{IH}min = 2.0 V V_{IH}max = 3.6 V V_{OL}max = 0.4 V V_{OH}min = 2.4 V	1.8 V power domain for RGMII. 1.8/3.3 V power domain for RMII. If unused, keep them open.
RGMII/RMII_CTL_RX	74	DI	RGMII/RMII receive control		
RGMII/RMII_CLK	75	DI	RGMII/RMII clock		
RGMII/RMII_RX_0	76	DI	RGMII/RMII receive data bit 0		
RGMII/RMII_TX_0	77	DO	RGMII/RMII transmit data bit 0		
RGMII/RMII_TX_1	78	DO	RGMII/RMII transmit data bit 1		
RGMII_RX_2	79	DI	RGMII receive data bit 2	VDD_EXT	
RGMII_TX_2	80	DO	RGMII transmit data bit 2		
RGMII/RMII_CTL_TX	81	DO	RGMII/RMII transmit control	**1.8V RGMII/RMII:** V_{IL}min = -0.3 V V_{IL}max = 0.54 V	

				V_{IH}min = 1.26 V V_{IH}max = 2.0 V V_{OL}max = 0.2 V V_{OH}min = 1.6 V **3.3 V RMII：** V_{IL}min = -0.3 V V_{IL}max = 0.8 V V_{IH}min = 2.0 V V_{IH}max = 3.6 V V_{OL}max = 0.4 V V_{OH}min = 2.4 V	
RGMII_RX_3	82	DI	RGMII receive data bit 3	VDD_EXT	
RGMII_CK_TX	83	DO	RGMII transmit clock		
RGMII_TX_3	84	DO	RGMII transmit data bit 3		
RGMII/RMII_INT	120	DI	RGMII/RMII interrupt input	**1.8V RGMII/RMII：** V_{IL}min = -0.3 V V_{IL}max = 0.54 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V V_{OL}max = 0.2 V V_{OH}min = 1.6 V **3.3 V RMII：** V_{IL}min = -0.3 V V_{IL}max = 0.8 V V_{IH}min = 2.0 V V_{IH}max = 3.6 V V_{OL}max = 0.4 V V_{OH}min = 2.4 V	
RGMII/RMII_MD_IO	121	DIO	RGMII/RMII management data input/output		
RGMII/RMII_MD_CLK	122	DO	RGMII/RMII management data clock		
RGMII/RMII_RST_N	119	DO	RGMII/RMII reset PHY chip	VDD_EXT	1.8 V power domain. Cannot be pulled high before module's successful power-on.
Analog Audio Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

SPK_N	123	AO	Analog audio differential output channel (-)		
SPK_P	124	AO	Analog audio differential output channel (+)		
MIC_P	125	AI	Microphone input channel (+)		
MIC_N	126	AI	Microphone input channel (-)		
MICBIAS	140	PO	Microphone bias voltage		
Other Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	115	DI	Forces the module to enter download mode	VDD_EXT	1.8 V power domain. Active High. It is recommended to reserve test points.
WAKEUP_IN*	1	DI	Wake up the module		1.8 V power domain. If unused, keep it open.
AP_READY*	2	DI	Application processor ready		1.8 V power domain. If unused, keep it open.
W_DISABLE#	4	DI	Airplane mode control	VDD_EXT	1.8 V power domain. Pull-up by default. In low voltage level, module can enter into airplane mode. If unused, keep it open.
RESERVED Pins					
Pin Name	**Pin No.**				**Comment**
RESERVED	18, 43, 47, 55, 113, 114, 116，117, 128, 137–139, 141–144				Keep these pins unconnected.

2.6. EVB Kit

To help you develop applications with the module, Quectel supplies an evaluation board (EVB) with accessories to control or test the module. For more details, see ***document [1]***.

3 Operating Characteristics

3.1. Operating Modes

The table below outlines operating modes of the module.

Table 7: Overview of Operating Modes

Mode	Details	
Full Functionality Mode	Idle	Software is active. The module is registered on the network and ready to send and receive data.
	Voice/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rate.
Minimum Functionality Mode	**AT+CFUN=0** command can set the module to a minimum functionality mode. In this case, both RF function and (U)SIM card will be invalid.	
Airplane Mode	**AT+CFUN=4** command or W_DISABLE# pin can set the module to airplane mode. In this case, RF function will be invalid.	
Sleep Mode	In this mode, current consumption of the module will be reduced to the minimal level. In this mode, the module can still receive paging, SMS, voice call and TCP/UDP data from network.	
Power Down Mode	In this mode, the VBAT power supply is constantly turned on and the software stops working.	

NOTE

For more details about the AT command, see ***document [2]***.

3.2. Sleep Mode

In sleep mode, the module can reduce power consumption to a very low level, the following section describes power saving procedures of EC200A series module.

3.2.1. UART Application

If the host communicates with module via UART interface, the following preconditions should be met to enable the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Drive MAIN_DTR to high level.
- Ensure the USB_VBUS is kept at low level, or kept open.

The following figure shows the connection between the module and the host.

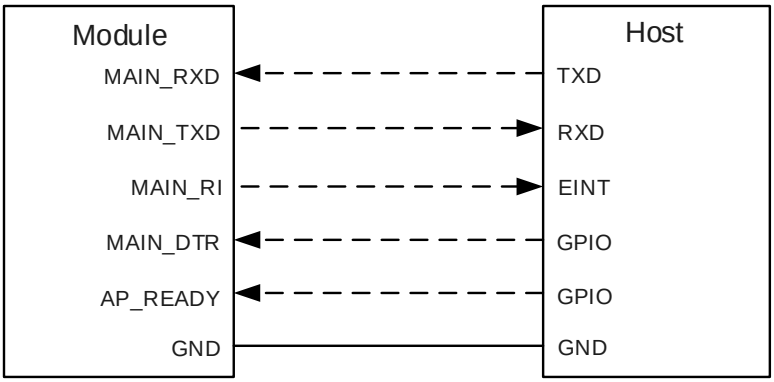


Figure 3: Sleep Mode Application via UART

- Driving MAIN_DTR to low level by host will wake up the module.
- When the module has a URC to report, the URC will trigger the behavior of MAIN_RI pin. Please refer to ***Chapter 4.12*** for details about MAIN_RI behavior.

3.2.2. USB Application with USB Remote Wakeup Function

If the host supports USB Suspend/Resume and remote wakeup functions, the following three preconditions must be met to let the module enter sleep mode.

- Execute **AT+QSCLK=1** command to enable the sleep mode.
- Ensure the MAIN_DTR is kept at high level or kept open.
- The host's USB bus, which is connected with the module's USB interface, enters Suspend state.

The following figure shows the connection between the module and the host.

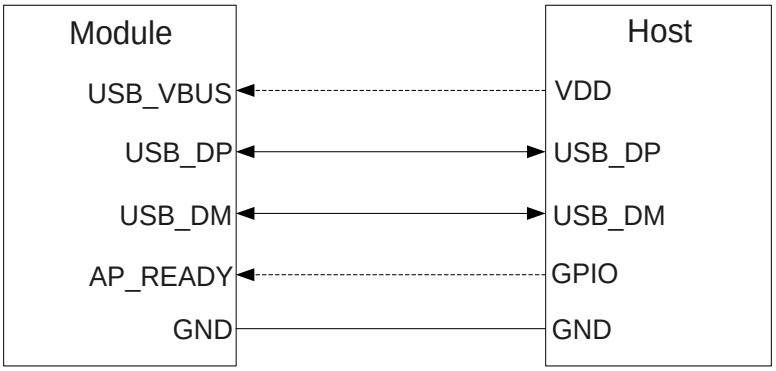


Figure 4: Sleep Mode Application with USB Remote Wakeup

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, the module will send remote wakeup signals via USB bus to wake up the host.

3.2.3. USB Application without USB Remote Wakeup Function

If the host supports USB Suspend/Resume, but does not support remote wakeup function, the MAIN_RI signal is needed to wake up the host.

There are three preconditions to let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable the sleep mode.
- Ensure the MAIN_DTR is held at high level or keep it open.
- The host's USB bus, which is connected with the module's USB interface, enters Suspend state.

The following figure shows the connection between the module and the host.

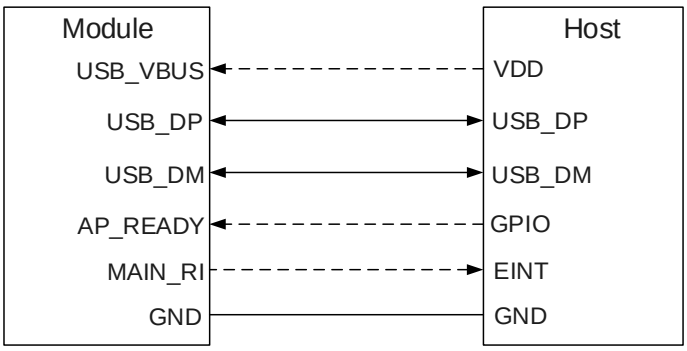


Figure 5: Sleep Mode Application with MAIN_RI

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, the URC will trigger the behavior of MAIN_RI pin. Please refer to ***Chapter 4.12*** for details about MAIN_RI behavior.

3.2.4. USB Application without USB Suspend Function

If the host does not support USB Suspend function, please disconnect USB_VBUS with additional control circuit to let the module enter into sleep mode.

- Execute **AT+QSCLK=1** command to enable the sleep mode.
- Ensure the MAIN_DTR is held at high level or keep it open.
- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

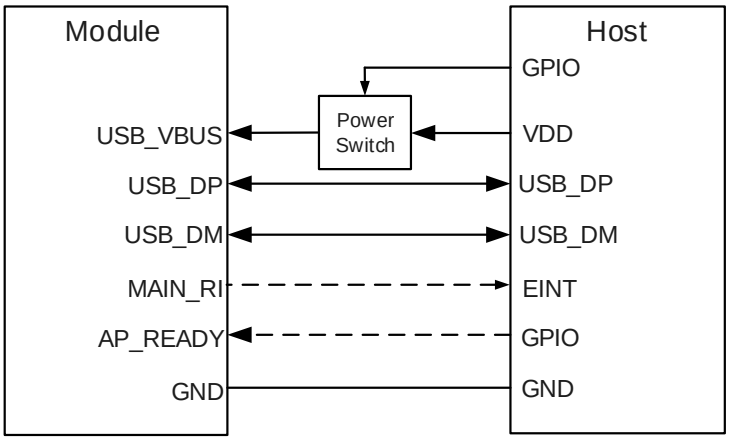


Figure 6: Sleep Mode Application without Suspend Function

Turn on the power switch and supply power to USB_VBUS will wake up the module.

NOTE

Please pay attention to the level match shown in dotted line between the module and the host.

3.3. Airplane Mode

When the module enters into airplane mode, the RF function will be disabled, and all AT commands related to it will be inaccessible. This mode can be set via the following ways.

Hardware:

The W_DISABLE# pin is pulled up by default. Its control function for airplane mode is disabled by default, and **AT+QCFG="airplanecontrol",1** can be used to enable the function. Driving the pin to low level can make the module enter airplane mode.

Software:

AT+CFUN=<fun> command provides choices of the functionality level through setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0:** Minimum functionality mode (Both (U)SIM and RF functions are disabled.).
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** Airplane mode (RF function is disabled.).

NOTE

For more details about AT command, see ***document [2]***.

3.4. Power Supply

3.4.1. Power Supply Pins

The module provides four VBAT pins dedicated to the connection with the external power supply. There are two separate voltage domains for VBAT.

- Two VBAT_RF pins for module's RF part
- Two VBAT_BB pins for module's baseband part

The following table shows the details of power supply and GND pins.

Table 8: Pin Definition of Power Supply

Pin Name	Pin No.	I/O	Description	Comment
VBAT_BB	59、60	PI	Power supply for the module's baseband part	It must be provided with sufficient current up to 0.8 A.
VBAT_RF	57、58	PI	Power supply for the module's RF part	It must be provided with sufficient current up to 2.0 A.

VDD_EXT	7	PO	Provide 1.8 V for external circuit	It can provide a pull-up power to the external GPIO. If unused, keep it open.

3.4.2. Reference Design for Power Supply

The performance of the module largely depends on the power source. The power supply of the module should be able to provide sufficient current of 2.8 A at least. If the voltage drops between input and output is not too high, it is suggested that an LDO should be used to supply power to the module. If there is a big voltage difference between input and the desired output VBAT, a buck converter is preferred as the power supply.

The following figure shows a reference design for +5 V input power source. The design uses the LDO MIC29302WU from Micrel company. The typical output of the power supply is about 3.8 V and the maximum load current is 3.0 A.

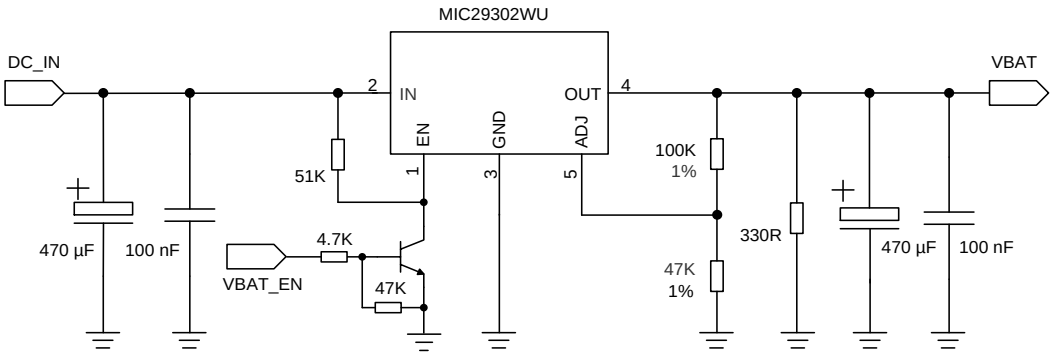


Figure 7: Reference Design of Power Supply

NOTE

It is recommended to design switch control for power supply.

3.4.3. Requirements for Voltage Stability

The power supply range of the module is from 3.4 V to 4.5 V. Please make sure the input voltage will never drop below 3.4 V.

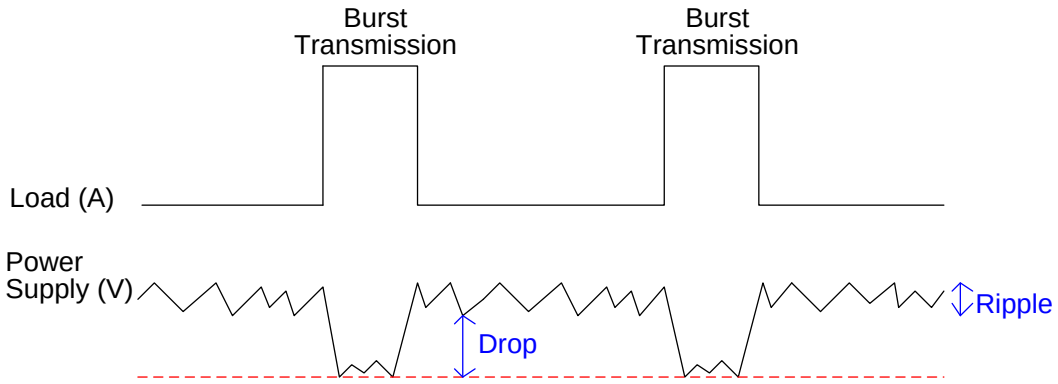


Figure 8: Power Supply Limits during Burst Transmission

To decrease voltage drop, a bypass capacitor of about 100 µF with low ESR (ESR = 0.7 Ω) should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to the VBAT_BB and VBAT_RF pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT_BB trace should be no less than 1 mm; and the width of VBAT_RF trace should be no less than 2 mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, in order to ensure the stability of power source, it is suggested that a TVS diode of which reverse stand-off voltage is 4.7 V and peak pulse power is up to 2550 W should be used. The following figure shows the star structure of the power supply.

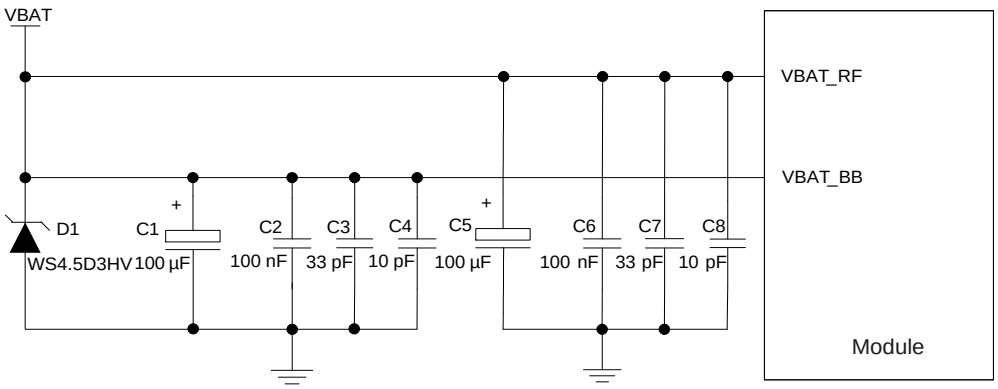


Figure 9: Star Structure of the Power Supply

3.5. Turn On

3.5.1. Turn on the Module with PWRKEY

Table 9: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	21	DI	Turn on/off the module	VBAT power domain. Active low.

When the module is in power down mode, it can be turned on to normal mode by driving the PWRKEY pin to a low level for at least 500 ms. It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

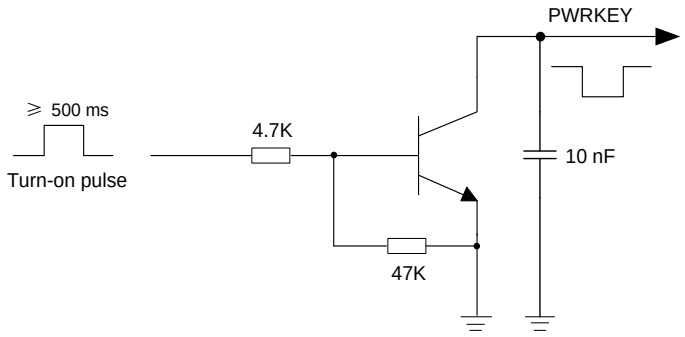


Figure 10: Reference Circuit of Turning on the Module Using Driving Circuit

The other way to control the PWRKEY is using a button directly. When pressing the button, electrostatic strike may generate from finger. Therefore, an ESD device should be placed near the button for electrostatic protection. The reference circuit is as follows.

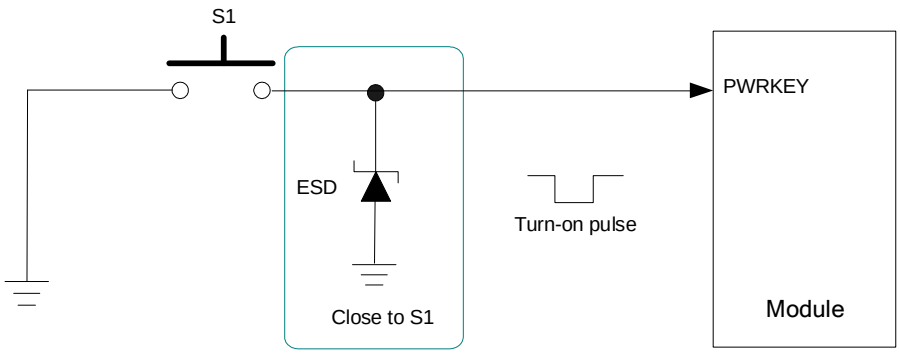


Figure 11: Reference Circuit of Turning on the Module with Button

The power-up scenario is illustrated in the following figure.

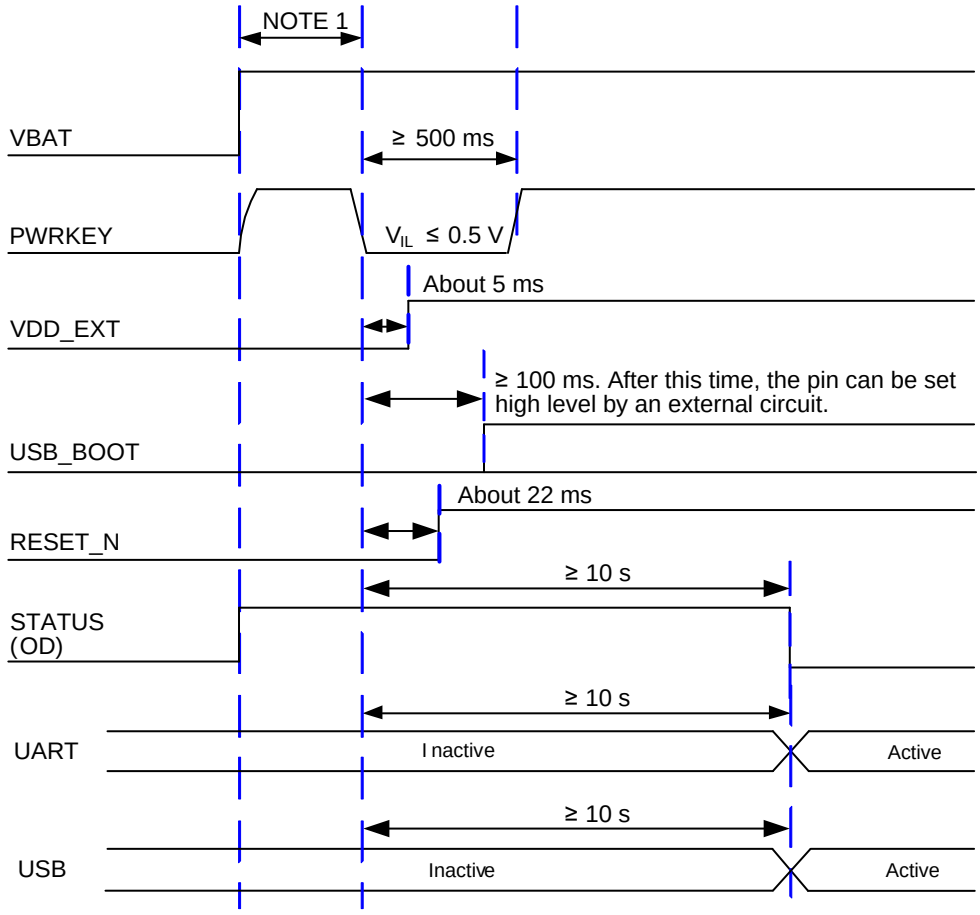


Figure 12: Power-up Timing

NOTE

1. Make sure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time difference between powering up VBAT and pulling down PWRKEY pin is no less than 450 ms.
2. PWRKEY can be pulled down directly to GND with a recommended 4.7 kΩ resistor if module needs to be powered on automatically and shutdown is not needed.

3.6. Turn Off

The following procedures can be used to turn off the module:

3.6.1. Turn off the Module with PWRKEY

Driving the PWRKEY to a low-level voltage for at least 650 ms, then the module will execute power-down procedure after the PWRKEY is released. The timing of turning off the module is illustrated in the following figure.

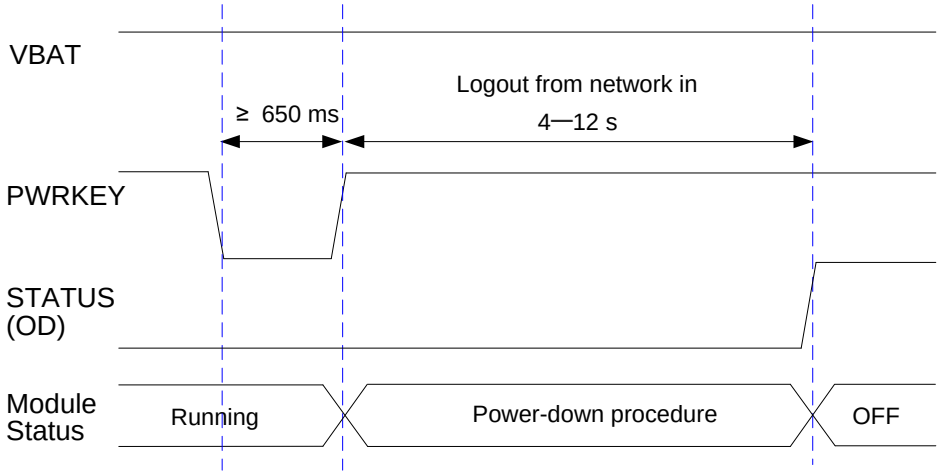


Figure 13: Timing of Turning off Module

During the turn-off process, the module needs to log out from network. The logout time is related to the current network state, It is measured to take about 4 to 12 s. Therefore, it is recommended to power off or restart the module after 12 s to ensure that the important software data is saved before completely shut down.

3.6.2. Turn off the Module with AT Command

It is safe to use **AT+QPOWD** command to turn off the module, which is equal to turn off the module via PWRKEY Pin.

Please refer to ***document [2]*** for details about **AT+QPOWD** command.

NOTE

1. To avoid damaging the data of internal flash, do not switch off the power supply when the module works normally. Only after shutting down the module with PWRKEY or AT command can you cut

off the power supply.
2. When turning off module with the AT command, please keep PWRKEY at high level after the execution of the command. Otherwise, the module will be turned on again after successfully turn-off.

3.7. Reset

The module can be reset by driving the RESET_N low for at least 300 ms and then releasing it. The RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 10: Pin Definition of RESET

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	20	DI	Reset the module	1.8 V power domain. Active low after turn-on.

The recommended circuit is equal to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

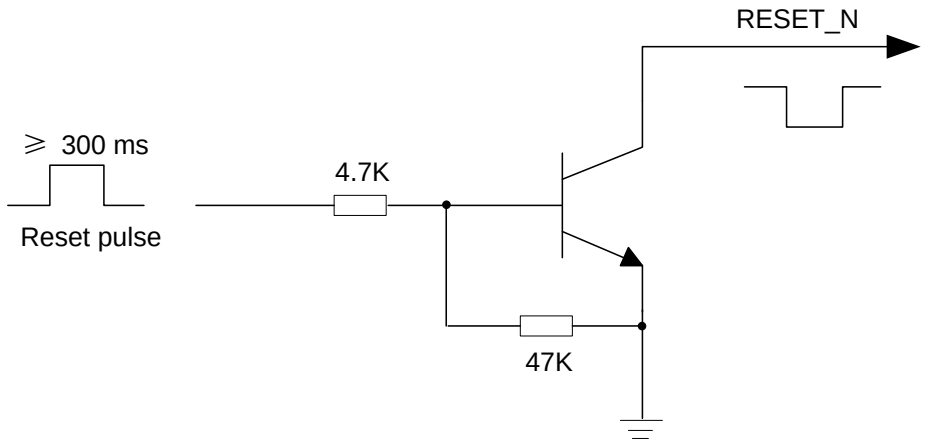


Figure 14: Reference Circuit of RESET_N with Driving Circuit

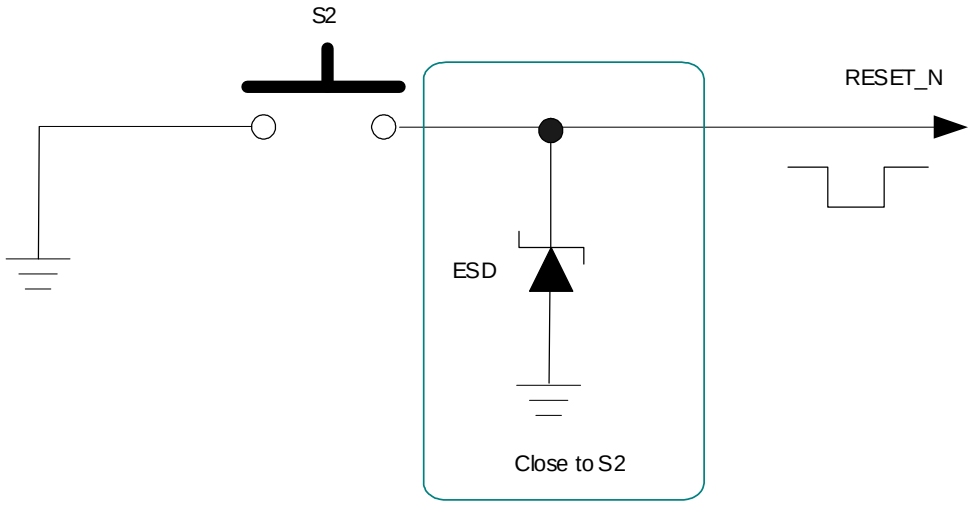


Figure 15: Reference Circuit of RESET_N with Button

The timing of resetting module is illustrated in the following figure.

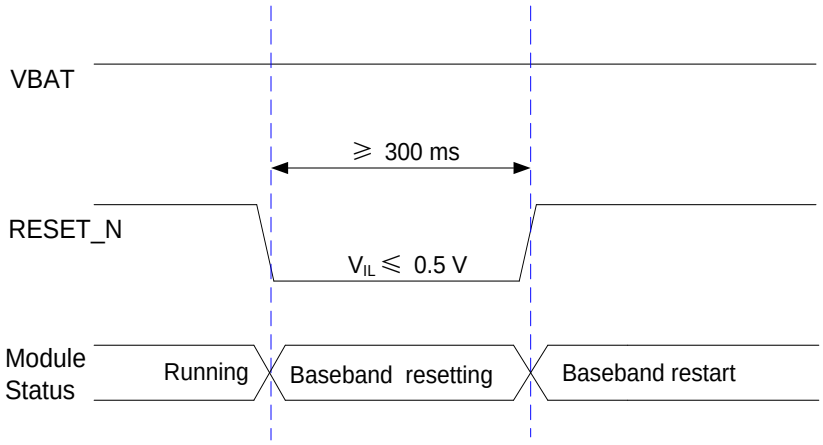


Figure 16: Timing of Resetting Module

NOTE

1. Please ensure that there is no large capacitance with the max value exceeding 10 nF on PWRKEY and RESET_N pins.
2. RESET_N only resets the internal baseband chip of the module and does not reset the power management chip.

4 Application Interfaces

4.1. USB Interface

EC200A series provides one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports full-speed (12 Mbps) and high-speed (480 Mbps) modes. The USB interface can only serve as a slave device and is used for AT command communication, data transmission, software debugging and firmware upgrade. The following table shows the pin definition of USB interface.

Table 11: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	71	AI	USB connection detect	Typ. 5.0 V. If unused, keep it open.
USB_DP	69	AIO	USB differential data (+)	90 Ω differential impedance. USB 2.0 compliant. If unused, keep it open.
USB_DM	70	AIO	USB differential data (-)	

For more details about the USB 2.0 specifications, please visit http://www.usb.org/home.

It is recommended to reserve test points for debugging and firmware upgrade in your designs. The following figure shows a reference circuit of USB interface.

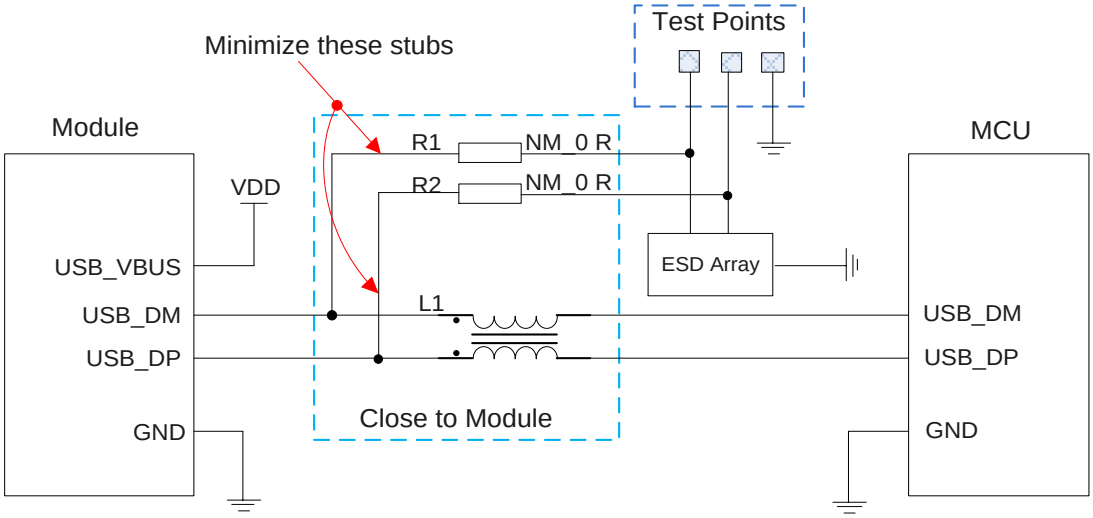


Figure 17: Reference Circuit of USB Interface

A common mode choke L1 is recommended to be added in series between the module and your MCU in order to suppress EMI spurious transmission. Meanwhile, the 0 Ω resistors (R1 and R2) should be added in series between the module and the test points so as to facilitate debugging, and the resistors are not mounted by default. In order to ensure the integrity of USB data line signal, L1, R1 and R2 components must be placed close to the module, and also resistors R1 and R2 should be placed close to each other. The extra stubs of trace must be as short as possible.

The following principles should be complied with when designing the USB interface, to meet USB specifications.

- It is important to route the USB signal traces as differential pairs with ground surrounded. The impedance of USB differential trace is 90 Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices, PCIe and RF signal traces. It is important to route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below.
- Junction capacitance of the ESD protection device might cause influences on USB data lines, so please pay attention to the selection of the device. Typically, the stray capacitance should be less than 2 pF for USB.
- If possible, reserve a 0 Ω resistor on USB_DP and USB_DM lines respectively.

For more details about the USB specifications, please visit http://www.usb.org/home.

4.2. USB_BOOT Interface

The module provides a USB_BOOT pin. You can pull up USB_BOOT to VDD_EXT before powering on the module, thus the module will enter emergency download mode when powered on. In this mode, the module supports firmware upgrade over USB interface.

Table 12: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	115	DI	Forces the module to enter download mode	1.8 V power domain. Active high. It is recommended to reserve test points.

The following figure shows a reference circuit of USB_BOOT interface.

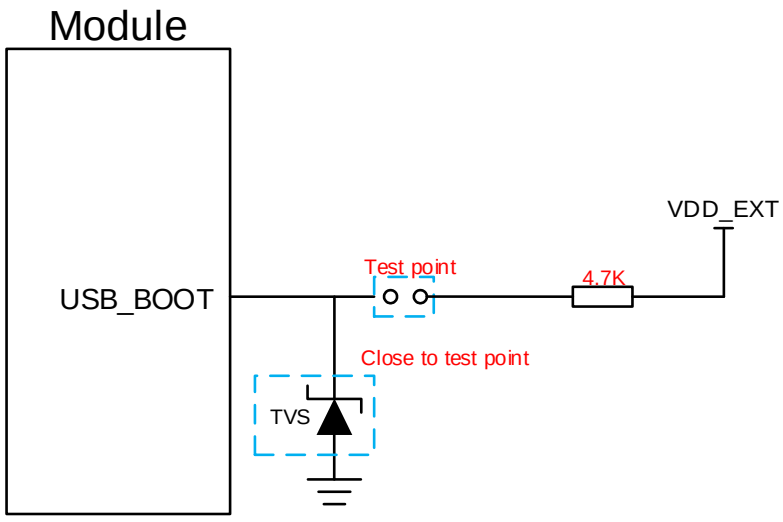


Figure 18: Reference Circuit of USB_BOOT Interface

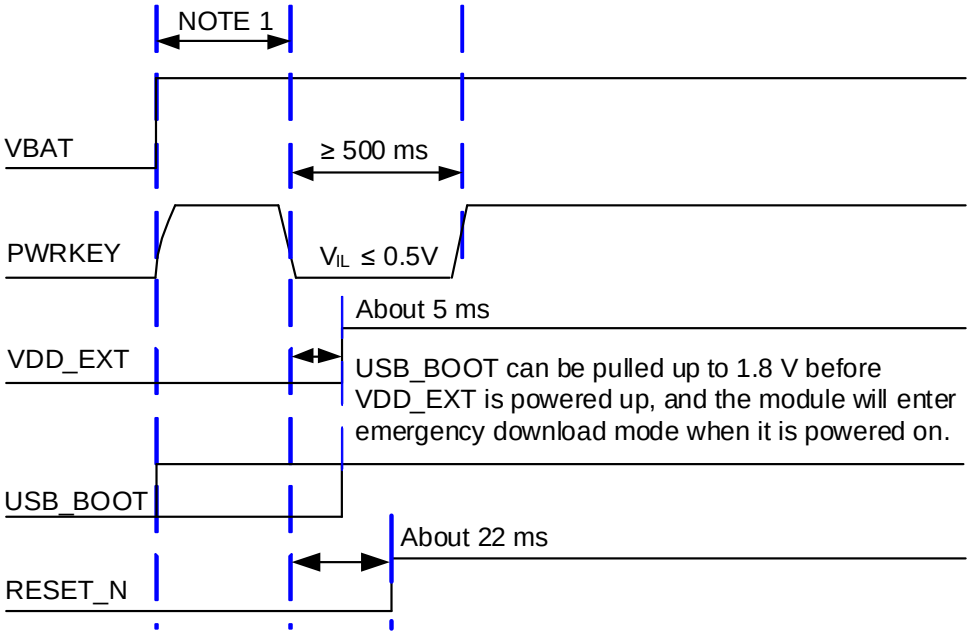


Figure 19: Timing Sequence for Entering Emergency Download Mode

NOTE

1. Please make sure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time between powering up VBAT and pulling down PWRKEY pin is no less than 450 ms.
2. When using MCU to control module to enter the emergency download mode, please follow the above timing sequence. It is not recommended to pull up USB_BOOT to 1.8 V before powering up VBAT. Directly connect the test points as shown in ***Figure 18*** can manually force the module into download mode.
3. USB_BOOT cannot be pulled up before module is turned on successfully.

4.3. (U)SIM Interface

The (U)SIM interface circuitry meets ETSI and IMT-2000 requirements. Both 1.8 V and 3.0 V (U)SIM cards are supported.

Table 13: Pin Definition of (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_VDD	14	PO	(U)SIM card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM_DATA	15	DIO	(U)SIM card data	
USIM_CLK	16	DO	(U)SIM card clock	
USIM_RST	17	DO	(U)SIM card reset	
USIM_DET	13	DI	(U)SIM card hot-plug detect	1.8 V power domain. If unused, keep it open.
USIM_GND	10		Dedicated ground for (U)SIM card	

The module supports (U)SIM card hot-plug via the USIM_DET pin, The function supports low level and high level detections. By default, It is disabled, and can be configured via **AT+QSIMDET** command. Please refer to ***document [2]*** for details about the command.

The reference circuit of the 8-pin (U)SIM interface is as follows.

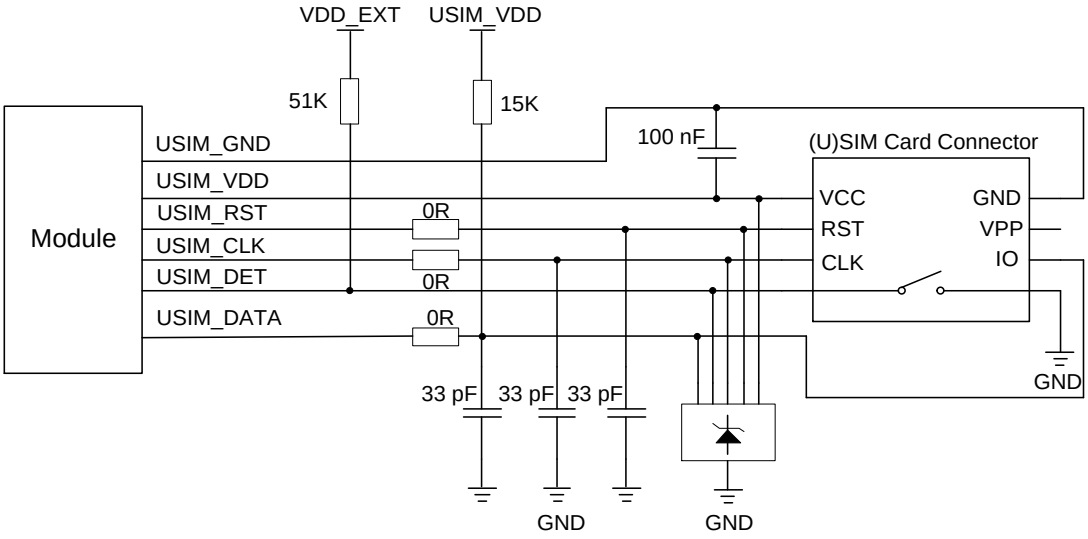


Figure 20: Reference Circuit of (U)SIM Interface with an 8-pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, please keep USIM_DET unconnected. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

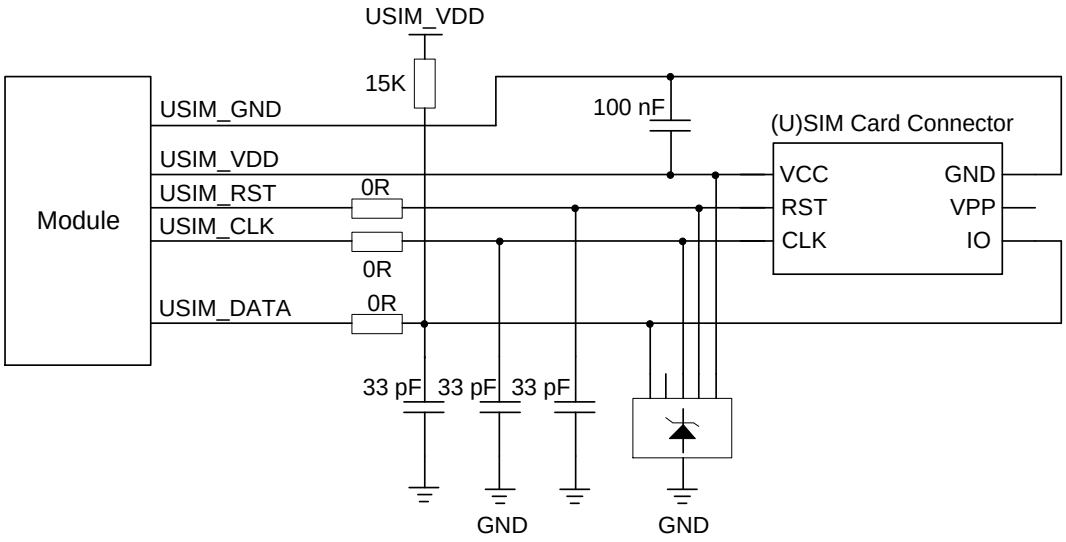


Figure 21: Reference Circuit of (U)SIM Interface with a 6-pin (U)SIM Card Connector

In order to enhance the reliability and availability of the (U)SIM card in applications, please follow the criteria below in (U)SIM circuit design.

- Keep (U)SIM card connector as close as possible to the module. Keep the trace length as less than 200 mm as possible.
- Keep (U)SIM card signal traces away from RF and VCC traces.
- USIM_VDD maximum bypass capacitor does not exceed 1uF.
- Ensure the ground between the module and the (U)SIM card connector short and wide. Keep the trace width of ground and USIM_VDD no less than 0.5 mm to maintain the same electric potential.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with ground surrounded.
- In order to offer good ESD protection, it is recommended to add an ESD protection component whose parasitic capacitance should not be more than 15 pF. The 0 Ω resistors should be added in series between the module and the (U)SIM card to facilitate debugging. The 33 pF capacitors on the USIM_DATA, USIM_CLK and USIM_RST trances are used for filtering interference. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA can improve anti-jamming capability of the (U)SIM card. If the (U)SIM card traces are too long, or the interference source is relatively close, it is recommended to add a pull-up resistor near the (U)SIM card connector.

4.4. PCM and I2C Interfaces

The module provides one Pulse Code Modulation (PCM) digital interface for audio design, which supports the primary mode (short frame synchronization) and the module works as both master and slave* device.

The module can only be used as primary devices in applications related to I2C interfaces and does not support multi-host mode. It conforms to the I2C bus protocol specification (100/400 kHz).

In short frame mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, the PCM interface supports 256 kHz, 512 kHz, 1024, 2048 kHz PCM_CLK at 8 kHz PCM_SYNC, and also supports 4069 kHz PCM_CLK at 16 kHz PCM_SYNC.

The module supports a 16-bit linear encoding format. The following figure shows the sequence diagram of short frame mode. (PCM_SYNC = 8 kHz, PCM_CLK = 2048 kHz).

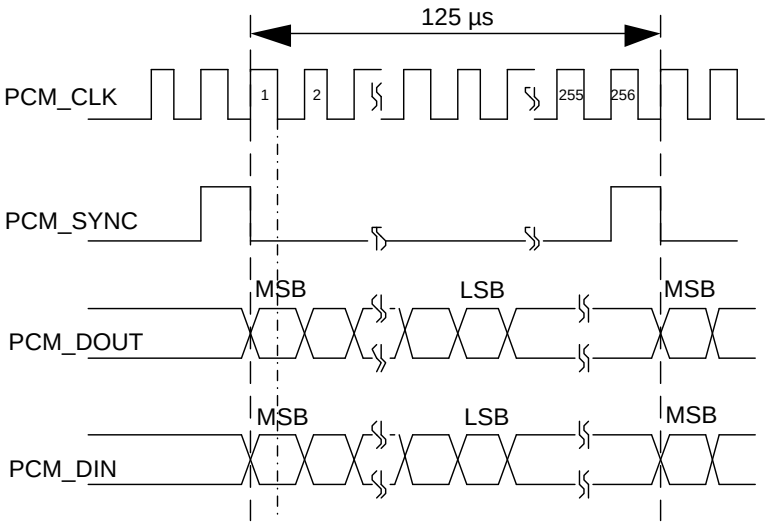


Figure 22：Timing Sequence for Short Frame Mode

Table 14: Pin Definition of PCM Interface

Pin Name	Pin No.	I/O	Description	Comment
PCM_SYNC	26	DIO	PCM data frame sync	1.8 V power domain. When the module is the master device, this pin is in the output state while when the module is used
PCM_CLK	27	DIO	PCM clock	

				as a slave* device, it is in the input state. If unused, keep it open.
PCM_DIN	24	DI	PCM data input	1.8 V power domain. If unused, keep them open.
PCM_DOUT	25	DO	PCM data output	

Table 15: Pin Definition of I2C Interface

Pin Name	Pin No.	I/O	Description	Comment
I2C_SCL	41	OD	I2C serial clock	Used for external codec. An external 1.8 V pull-up resistor is needed.
I2C_SDA	42	OD	I2C serial data	

Clock and mode can be configured by AT command, and the default configuration is short frame synchronization format with 2048 kHz PCM_CLK and 8 kHz PCM_SYNC.

The following is a reference design for the PCM and I2C interfaces with external Codec chip.

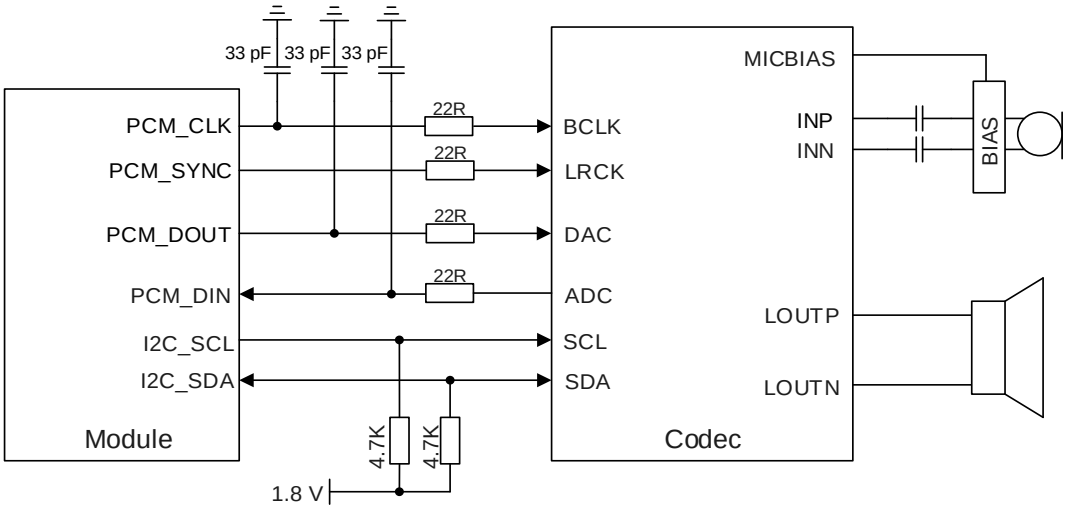


Figure 23: PCM and I2C Interface Circuit Reference Design

NOTE

It is recommended to reserve the RC (R = 22 Ω, C = 33 pF) circuit on the PCM signal line and the capacitor should be placed close to the module, especially on PCM_CLK.

4.5. SPI Interface

The module provides one SPI interface that supports master mode with a maximum clock frequency of 52 MHz.

Table 16: Pin Definition of SPI Interface

Pin Name	Pin No.	I/O	Description	Comment
SPI_CLK	40	DO	SPI clock	1.8 V power domain. If unused, keep them open.
SPI_CS	37	DO	SPI chip select	
SPI_DIN	39	DI	SPI data input	
SPI_DOUT	38	DO	SPI data output	

NOTE

When SPI is connected to the SLIC chip SI32185, you need to use pin 3 of the module as RESET_SLIC to connect to pin 18 of SI32185, use pin 4 of the module as INT_SLIC to connect to pin 6 of SI32185, and you need to change the GPIO configuration of module pin 3 and 4 of the module.

4.6. Analog Audio Interfaces

The module provides one analog audio input channel and one analog audio output channel. Pin definition is shown in the following table.

Table 17: Pin Definition of Analog Audio Interfaces

Channel	Pin Name	Pin No.	I/O	Description
AIN	MICBIAS	140	PO	Microphone bias voltage
	MIC_P	125	AI	Microphone input channel (+)
	MIC_N	126		Microphone input channel (-)
AOUT	SPK_P	124	AO	Analog audio differential output channel (+)

SPK_N	123	Analog audio differential output channel (-)

- AIN channels are differential inputs and are used for microphone input. Electret microphones are usually used.
- AOUT channel is a differential output, usually used for earpiece.

4.6.1. Notes on Audio Interface Design

It is recommended to use the electret microphone with dual built-in capacitors (e.g. 10 pF and 33 pF) for filtering out RF interference, thus reducing TDD noise. The 33 pF capacitor is applied for filtering out RF interference when the module is transmitting at EGSM900. Without placing this capacitor, TDD noise could be heard. The 10 pF capacitor here is used for filtering out RF interference at DCS1800. Please note that the resonant frequency point of a capacitor largely depends on the material and production technique. Therefore, you would have to discuss with their capacitor vendors to choose the most suitable capacitor for filtering out high-frequency noises.

The severity degree of the RF interference in the voice channel during GSM transmitting largely depends on the application design. In some cases, EGSM900 TDD noise is more severe; while in other cases, DCS1800 TDD noise is more obvious. Therefore, a suitable capacitor can be selected based on the test results. The filter capacitors on the PCB should be placed as close to the audio devices or audio interfaces as possible, and the traces should be as short as possible. They should go through the filter capacitors before arriving at other connection points.

In order to decrease radio or other signal interference, RF antennas should be placed away from audio interfaces and audio traces. Power traces cannot be parallel with and also should be far away from the audio traces.

The differential audio traces must be routed according to the differential signal layout rule.

4.6.2. Microphone Interface Circuit

The microphone interface reference circuit is shown below

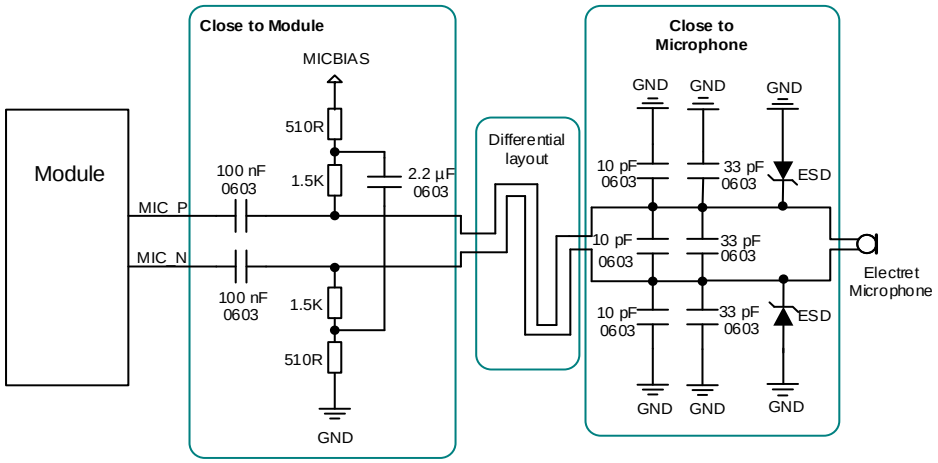


Figure 24: Microphone Interface Reference Circuit

NOTE

MIC channel is sensitive to ESD, so it is not recommended to remove the ESD components used for protecting the MIC.

4.6.3. Earpiece Interface Circuit

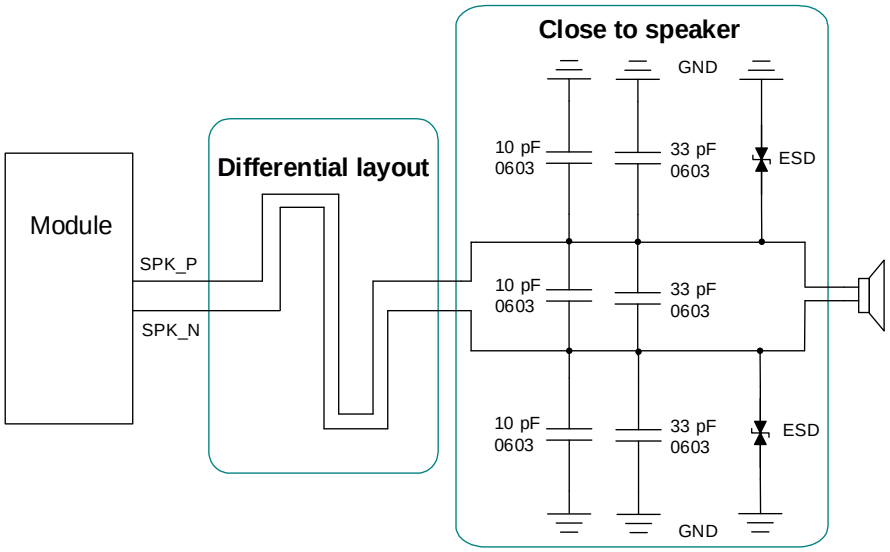


Figure 25: Earpiece Interface Reference Circuit

4.7. UART Interface

The module provides two UART interfaces: the main UART interface and the debug UART interface. The following shows their features.

- The main UART interface supports 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps, 921600 bps baud rates, and the baud rate is 115200 bps by default. This interface is used for data transmission and AT command communication. Also, it supports RTS and CTS hardware flow control.
- The debug UART interface supports 115200 bps baud rate. It is used for the output of partial logs.

Table 18: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
MAIN_RI	62	DO	Main UART ring indication	1.8 V power domain. If unused, keep them open.
MAIN_DCD	63	DO	Main UART data carrier detect	
MAIN_CTS	64	DO	DTE clear to send signal from DCE (Connect to DTE's CTS)	
MAIN_RTS	65	DI	DTE request to send signal to DCE (Connect to DTE's RTS)	
MAIN_DTR	66	DI	Main UART data terminal ready	
MAIN_RXD	68	DI	Main UART receive	
MAIN_TXD	67	DO	Main UART transmit	

Table 19: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_RXD	11	DI	Debug UART transmit	1.8 V power domain. If unused, keep them open.
DBG_TXD	12	DO	Debug UART receive	

The module provides a 1.8 V UART interface. A level translator should be used if the application is equipped with a 3.3 V UART interface. A level translator TXS0108EPWR provided by *Texas Instruments* is recommended. The following figure shows a reference design.

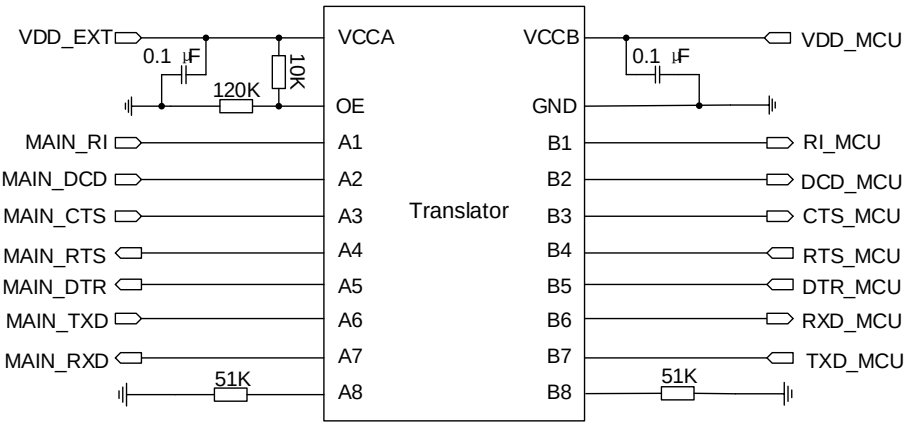


Figure 26: Reference Circuit with Translator Chip

Please visit http://www.ti.com for more information.

Another example with transistor circuit is shown as below. For the design of circuits shown in dotted lines, please refer to that shown in solid lines, but pay attention to the direction of connection.

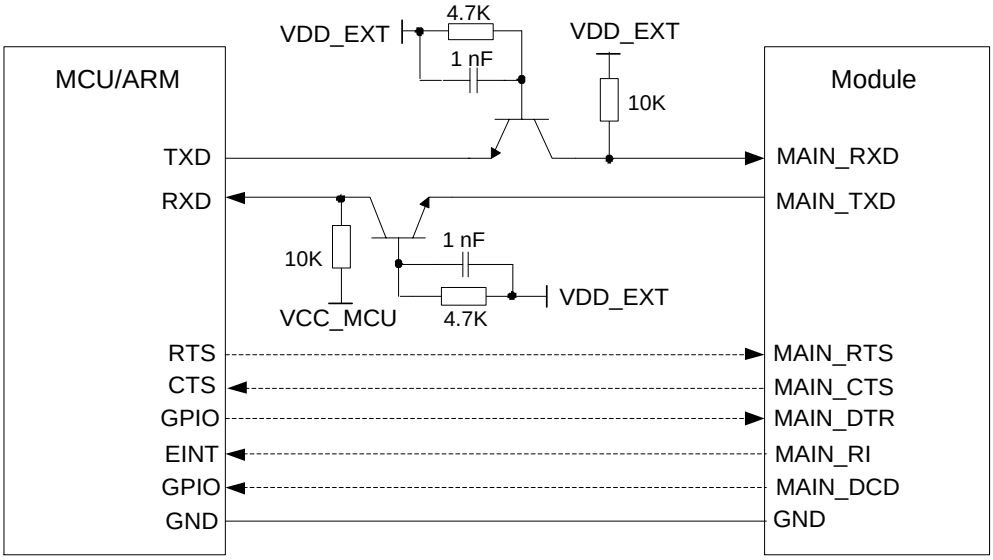


Figure 27: Reference Circuit with Transistor Circuit

NOTE

1. Transistor circuit solution is not suitable for applications with baud rates exceeding 460 kbps.
2. Please note that the module CTS is connected to the host CTS, and the module RTS is connected to the host RTS.

4.8. SD card Interface

The module provides one SD card interface which supports SD 3.0 protocol.

Table 20: Pin Definition of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment
SD_SDIO_CLK	32	DO	SD card SDIO clock	1.8/2.8 V power domain. If unused, keep them open.
SD_SDIO_CMD	33	DIO	SD card SDIO command	
SD_SDIO_DATA0	31	DIO	SD card SDIO bit 0	
SD_SDIO_DATA1	30	DIO	SD card SDIO bit 1	
SD_SDIO_DATA2	29	DIO	SD card SDIO bit 2	
SD_SDIO_DATA3	28	DIO	SD card SDIO bit 3	
SD_SDIO_VDD	34	PO	SD card SDIO power supply	
SD_DET*	23	DI	SD card hot-plug detect	1.8 V power domain. If unused, keep it open.

The following figure illustrates a reference design of SD card interface with the module.

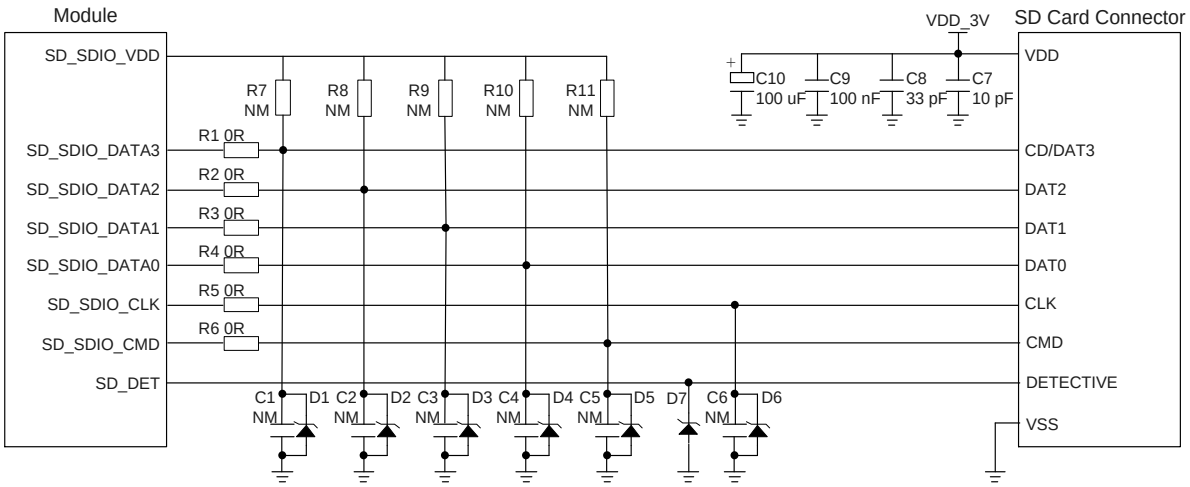


Figure 28: Reference Circuit of SD Card Interface

In SD card interface design, in order to ensure good communication performance with SD card, the following design principles should be complied with:

- The voltage range of SD card power supply VDD_3V is 2.7–3.6 V and a sufficient current up to 0.8 A should be provided. The maximum output current of SD_SDIO_VDD is 50 mA which can only be used for SDIO pull-up resistors, an externally power supply is needed for SD card.
- To avoid jitter of bus, resistors R7–R11 are needed to pull up the SDIO to SD_SDIO_VDD. Value of these resistors is among 10 kΩ to 100 kΩ and the recommended value is 100 kΩ. SD_SDIO_VDD should be used as the pull-up power.
- In order to improve signal quality, it is recommended to add 0 Ω resistors R1 to R6 in series between the module and the SD card. The bypass capacitors C1 to C6 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.
- In order to offer good ESD protection, it is recommended to add an ESD protection component on SD card pins near the SD card connector with junction capacitance less than 8 pF.
- It is important to route the SDIO signal traces with ground surrounded. The impedance of SDIO data trace is 50 Ω (±10 %).
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals, etc.
- It is recommended to keep the traces of SD_SDIO_CLK, SD_SDIO_DATA [0:3] and SD_SDIO_CMD with equal length (the difference among them is less than 1 mm) and the total routing length needs to be less than 50 mm.
- Make sure the adjacent trace spacing is two times of the trace width and the load capacitance of SDIO Bus should be less than 15 pF.

4.9. ADC Interface

The module provides two Analog-to-Digital Converter (ADC) interfaces. In order to improve the accuracy of ADC, the trace of ADC interfaces should be surrounded by ground.

Table 21: Pin Definition of ADC Interface

Pin Name	Pin No.	I/O	Description	Comment
ADC0	45	AI	General-purpose ADC interface	If unused, keep them open.
ADC1	44	AI		

The voltage value on ADC pins can be read via **AT+QADC=<port>** command:

- **AT+QADC=0:** read the voltage value on ADC0
- **AT+QADC=1:** read the voltage value on ADC1

For more details about the AT command, please refer to ***document [2]***.

The resolution of the ADC is up to 12 bits. The following table describes the characteristic of the ADC interface.

Table 22: Characteristics of ADC Interface

Name	Min.	Typ.	Max.	Unit
ADC0 Voltage Range	0	-	VBAT_BB	V
ADC1 Voltage Range	0	-	VBAT_BB	V
ADC Resolution	-	12	-	bits

NOTE

1. The input voltage of ADC should not exceed its corresponding voltage range.
2. It is prohibited to supply any voltage to ADC pin when VBAT is removed.
3. It is recommended to use resistor divider circuit for ADC application and the divider resistance should not exceed 100K.

4.10. RGMII*/RMII Interface

The module provides one RGMII/RMII interface that can be used to connect 100/1000 Mbps Ethernet PHYs.

Table 23: Pin Definition of RGMII/RMII Interface

Pin Name	Pin No.	I/O	Description	Comment
RGMII/RMII_RX_1	73	DI	RGMII/RMII receive data bit 1	1.8 V power domain for RGMII. 1.8/3.3 V power domain for RMII. If unused, keep them open.
RGMII/RMII_CTL_RX	74	DI	RGMII/RMII receive control	
RGMII/RMII_CLK	75	DI	RGMII/RMII clock	
RGMII/RMII_RX_0	76	DI	RGMII/RMII receive data bit 0	
RGMII/RMII_TX_0	77	DO	RGMII/RMII transmit data bit 0	

RGMII/RMII_TX_1	78	DO	RGMII/RMII transmit data bit 1	
RGMII_RX_2	79	DI	RGMII receive data bit 2	
RGMII_TX_2	80	DO	RGMII transmit data bit 2	
RGMII/RMII_CTL_TX	81	DO	RGMII/RMII transmit control	
RGMII_RX_3	82	DI	RGMII receive data bit 3	
RGMII_CK_TX	83	DO	RGMII transmit clock	
RGMII_TX_3	84	DO	RGMII transmit data bit 3	
RGMII/RMII_INT	120	DI	RGMII/RMII interrupt input	
RGMII/RMII_MD_IO	121	DIO	RGMII/RMII management data input/output	
RGMII/RMII_MD_CLK	122	DO	RGMII/RMII management data clock	
RGMII/RMII_RST_N	119	DO	RGMII/RMII reset	1.8 V power domain. Cannot be pulled high before module's successful power-on. If unused, keep it open.

The following figure shows a reference circuit of RGMII MAC (3.3 V power domain) to PHY interface (3.3 V power domain).

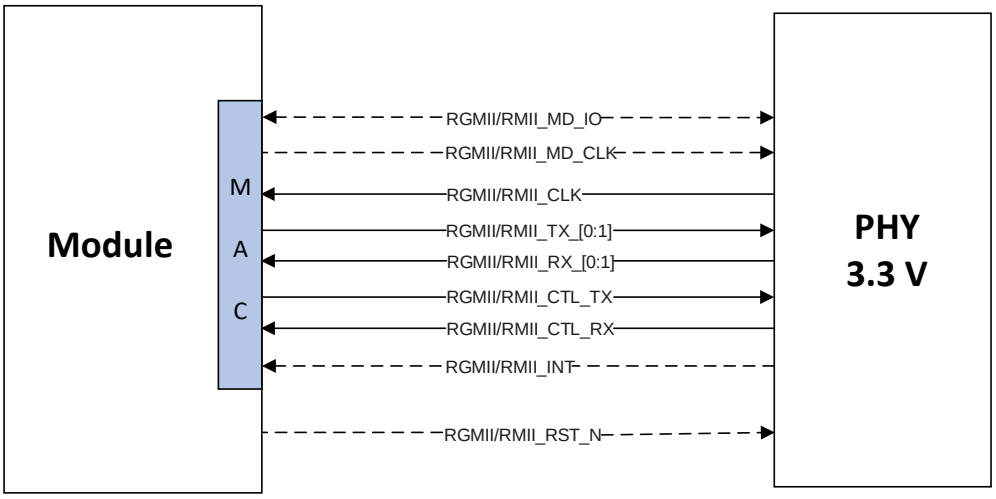


Figure 29: Reference Circuit of RMII to PHY Interface

The following figure shows a reference circuit of RGMII MAC (1.8 V power domain) to PHY (1.8 V power domain) interface.

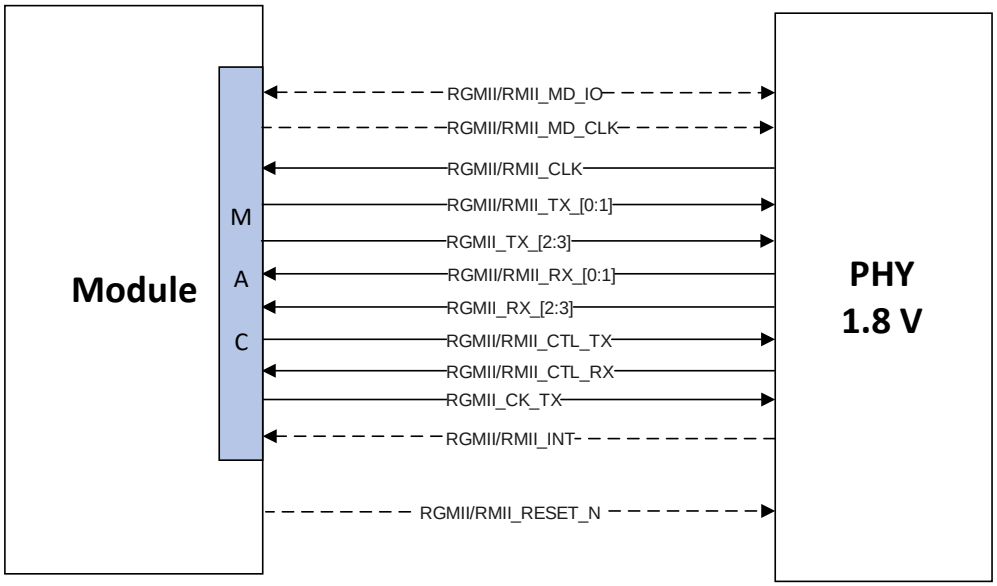


Figure 30: Reference Circuit of RGMII to PHY Interface

To enhance the reliability and availability of application designs, please follow the criteria below for RGMII/RMII circuit design:

- Keep RMII and RGMII data and control signals away from VBAT circuit, crystals, oscillators, magnetic devices and other sensitive signals such as RF circuits, analog signals, as well as noisy signals such as clock signals, DC-DC signals.

- The single-ended impedance of RGMII/RMII data trace is 50 Ω ±10 %.
- The length difference of RGMII/RMII_TX_[0:1], RGMII_TX_[2:3], RGMII/RMII_CTL_TX, RGMII_CK_TX should be less than 2 mm, and the space between the signal traces should be larger than 2 times of trace width. Similarly, The length difference of RGMII/RMII_RX_[0:1], RGMII_RX_[2:3], RGMII/RMII_CTL_RX, RGMII/RMII_CLK should be less than 2 mm, and the space between the signal traces should be larger than 2 times of trace width.
- Spacing between Tx bus and Rx bus is larger than 2.5 times of the trace width.
- Spacing between Tx bus or Rx bus is larger than 3 times of the trace width.

NOTE

Pay attention to the level match shown in dotted line.

4.11. Indication Signal

The pin definition of indication signal is as follows:

Table 24: Pin Definition of Indication Signal

Pin Name	Pin No.	I/O	Description	Comment
STATUS	61	OD	Indicate the module's operation status	1.8 V power domain. If unused, keep them open.
NET_MODE	5	DO	Indicate the module's network registration mode	
NET_STATUS	6	DO	Indicate the module's network activity status	
SLEEP_IND	3	DO	Indicate the module's sleep mode	

4.11.1. Network Status Indication

The network indication pins can be used to drive network status indication LEDs. The module provides two network indication pins: NET_MODE and NET_STATUS. The following tables describe pin definition and logic level changes in different network status.

Table 25: Working State of the Network Connection Status/Activity Indication

Pin Name	Status	Description
NET_MODE	Always High	Registered on LTE network
	Always Low	Others
NET_STATUS	Flicker slowly (200 ms High/1800 ms Low)	Network searching
	Flicker slowly (1800 ms High/200 ms Low)	Idle
	Flicker quickly (125 ms High/125 ms Low)	Data transfer is ongoing
	Always High	Voice calling

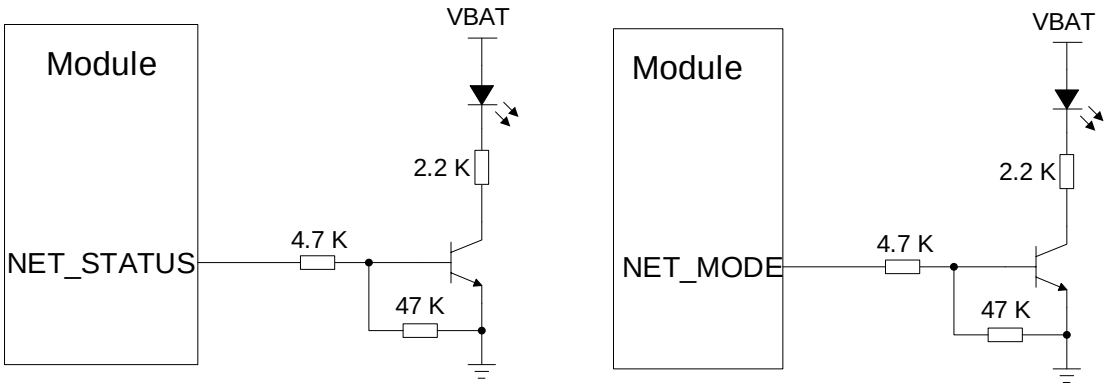


Figure 31: Reference Circuit of the Network Status Indication

4.11.2. STATUS

The STATUS pin is an open drain output for module's operation status indication. It can be connected to a GPIO of DTE with a pulled-up resistor, or as an LED indication circuit as below. When the module is turned on normally, the STATUS will present the low state. Except for this, the STATUS will present high-impedance state.

The following figure shows different circuit designs of STATUS, and you can choose either one according to the application demands.

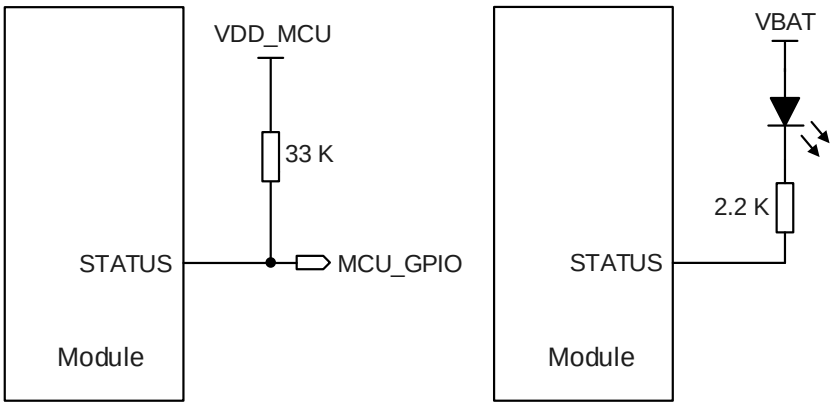


Figure 32: Reference Circuits of STATUS

NOTE

The status pin cannot be used as indication of module shutdown status when VBAT is removed.

4.12. Behaviors of the MAIN_RI

AT+QCFG="risignaltype","physical" can be used to configure MAIN_RI behaviors.

No matter on which port a URC is presented, the URC will trigger the behaviors of MAIN_RI pin.

NOTE

The URC can be outputted via UART port, USB AT port and USB modem port, which can be set by **AT+QURCCFG**. The default port is USB AT port.

In addition, MAIN_RI behavior can be configured flexibly. The default behavior of the MAIN_RI is shown as below.

Table 26: Behaviors of the MAIN_RI

State	Response
Idle	MAIN_RI keeps at high level
URC	MAIN_RI outputs 120 ms low pulse when a new URC returns

The MAIN_RI behavior can be changed via **AT+QCFG**. Please refer to ***document [2]*** for details.

4.13. WLAN_SDIO Interface

The module provides one low-power SDIO 3.0 interface and one control interface for WLAN design.

Table 27：Pin Definition of WLAN Interface

Pin Name	Pin No.	I/O	Description	Comment
WLAN_SLP_CLK*	118	DO	WLAN sleep clock	1.8 V power domain. If unused, keep them open.
WLAN_PWR_EN	127	DO	WLAN power supply enable control	
WLAN_SDIO_DATA3	129	DIO	WLAN SDIO data bit 3	
WLAN_SDIO_DATA2	130	DIO	WLAN SDIO data bit 2	
WLAN_SDIO_DATA1	131	DIO	WLAN SDIO data bit 1	
WLAN_SDIO_DATA0	132	DIO	WLAN SDIO data bit 0	
WLAN_SDIO_CLK	133	DO	WLAN SDIO clock	
WLAN_SDIO_CMD	134	DO	WLAN SDIO command	
WLAN_WAKE	135	DI	Wake up the host by an external Wi-Fi module	
WLAN_EN	136	DO	WLAN function enable control	

In WLAN SDIO interface design, in order to ensure good performance, the following design principles should be complied with:

- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO signal trace is 50 Ω ±10 %.
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, as well as noisy signals such as clock signals, DC-DC signals.
- It is recommended to keep the trace length difference between WLAN_SDIO_CLK, WLAN_SDIO_DATA and WLAN_SDIO_CMD less than 1 mm and the total routing length less than 50 mm.
- In order to improve the signal quality, the WLAN_SDIO_CLK signal trace needs to be connected with 15–24 Ω resistances near the module in series, and the distance from the WLAN_SDIO_CLK pin to the resistance needs to be less than 5 mm.
- The spacing between SDIO signals and other signals needs to be greater than twice the trace width, and the load capacitance of SDIO bus is less than 15 pF.

5 RF Specifications

5.1. Cellular Network

5.1.1. Antenna Interface & Frequency Bands

The pin definition of main antenna and Rx-diversity antenna interfaces is shown below.

Table 28: Pin Definition of Cellular Network Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_DRX	35	AI	Diversity antenna interface	50 Ω impedance.
ANT_MAIN	49	AIO	Main antenna interface	

Table 29: Operating Frequency of EC200A-CN

Operating Frequency	Transmit (MHz)	Receive (MHz)
EGSM900	880–915	925–960
DCS1800	1710–1785	1805–1880
WCDMA B1	1922–1978	2112–2168
WCDMA B5	826–847	871–892
WCDMA B8	882–913	927–958
LTE-FDD B1	1920–1980	2110–2170
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B5	824–849	869–894
LTE-FDD B8	880–915	925–960

LTE-TDD B34	2010–2025	2010–2025
LTE-TDD B38	2570–2620	2570–2620
LTE-TDD B39	1880–1920	1880–1920
LTE-TDD B40	2300–2400	2300–2400
LTE-TDD B41	2535–2675	2535–2675

NOTE

B41 only supports 140 MHz (2535–2675 MHz).

Table 30: Operating Frequency of EC200A-AU

Operating Frequency	Transmit (MHz)	Receive (MHz)
GSM850	824–849	869–894
EGSM900	880–915	925–960
DCS1800	1710–1785	1805–1880
PCS1900	1850–1910	1930–1990
WCDMA B1	1922–1978	2112–2168
WCDMA B2	1852–1908	1932–1988
WCDMA B4	1712–1753	2112–2153
WCDMA B5	826–847	871–892
WCDMA B8	882–913	927–958
LTE-FDD B1	1920–1980	2110–2170
LTE FDD B2	1850–1910	1930–1990
LTE-FDD B3	1710–1785	1805–1880
LTE FDD B4	1710–1755	2110–2155
LTE-FDD B5	824–849	869–894

LTE-FDD B7	2500–2570	2620–2690
LTE-FDD B8	880–915	925–960
LTE-FDD B28	703–748	758–803
LTE-FDD B66	1710–1780	2110–2180
LTE-TDD B40	2300–2400	2300–2400

Table 31: Operating Frequency of EC200A-EU

Operating Frequency	Transmit (MHz)	Receive (MHz)
EGSM900	880–915	925–960
DCS1800	1710–1785	1805–1880
WCDMA B1	1922–1978	2112–2168
WCDMA B5	826–847	871–892
WCDMA B8	882–913	927–958
LTE-FDD B1	1920–1980	2110–2170
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B5	824–849	869–894
LTE-FDD B7	2500–2570	2620–2690
LTE-FDD B8	880–915	925–960
LTE-FDD B20	832–862	791–821
LTE-FDD B28	703–748	758–803
LTE-TDD B38	2570–2620	2570–2620
LTE-TDD B40	2300–2400	2300–2400
LTE-TDD B41	2535–2675	2535–2675

Table 32: Operating Frequency of EC200A-EL

Operating Frequency	Transmit (MHz)	Receive (MHz)
WCDMA B1	1922~1978	2112~2168
WCDMA B5	826~847	871~892
WCDMA B8	882~913	927~958
LTE-FDD B1	1920~1980	2110~2170
LTE-FDD B3	1710~1785	1805~1880
LTE-FDD B5	824~849	869~894
LTE-FDD B7	2500~2570	2620~2690
LTE-FDD B8	880~915	925~960
LTE-FDD B20	832~862	791~821
LTE-FDD B28	703~748	758~803
LTE-TDD B38	2570~2620	2570~2620
LTE-TDD B40	2300~2400	2300~2400
LTE-TDD B41	2535~2675	2535~2675

5.1.2. Tx Power

The following table shows the RF output power of the module.

Table 33: Tx Power

Frequency	Max. Tx Power	Comments
GSM850	33 dBm ±2 dB	5 dBm ±5 dB
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
PCS1900	30 dBm ±2 dB	0 dBm ±5 dB
GSM850(8-PSK)	27 dBm ±3 dB	5 dBm ±5 dB

GSM900 (8-PSK)	27 dBm ±3 dB	5 dBm ±5 dB
DCS1800 (8-PSK)	26 dBm ±3 dB	0 dBm ±5 dB
PCS1900(8-PSK)	26 dBm ±3 dB	0 dBm ±5 dB
WCDMA B1/B2/B4/B5/B8	24 dBm +1/-3 dB	< -49 dBm
LTE-FDD B1/B2/B3/B4/B5/B7/B8/B20/B28/B66	23 dBm ±2 dB	< -39 dBm
LTE-TDD B34/B38/B39/B40/B41	23 dBm ±2 dB	< -39 dBm

NOTE

In GPRS 4 slots Tx mode, the maximum output power is reduced by 4 dB. The design conforms to the GSM specification as described in ***Chapter 13.16*** of 3GPP TS 51.010-1.

5.1.3. Rx Sensitivity

The following table shows conducted Rx sensitivity of the module.

Table 34: Conducted RF Receiving Sensitivity of EC200A-CN

Frequency	Receiving Sensitivity (Typ.)			3GPP Requirement (SIMO)
	Primary	Diversity	SIMO	
EGSM900	-109	-	-	-102 dBm
DCS1800	-107	-	-	-102 dBm
WCDMA B1	-109.4	-	-	-106.7 dBm
WCDMA B5	-109.7	-	-	-104.7 dBm
WCDMA B8	-110.2	-	-	-103.7 dBm
LTE-FDD B1	-98.1	-98.4	-101.3	-96.3 dBm
LTE-FDD B3	-97.1	-98.1	-100.8	-93.3 dBm
LTE-FDD B5	-98.9	-99.7	-101.9	-94.3 dBm
LTE-FDD B8	-97.4	-99.2	-101.9	-93.3 dBm
LTE-TDD B34	-96.6	-98.7	-100.5	-96.3 dBm

LTE-TDD B38	-96.7	-96.4	-98.9	-96.3 dBm
LTE-TDD B39	-97.6	-98	-100.3	-96.3 dBm
LTE-TDD B40	-97.4	-98.9	-101.4	-96.3 dBm
LTE-TDD B41	-95	-95.8	-99.1	-94.3 dBm

Table 35: Conducted RF Receiving Sensitivity of EC200A-AU

Frequency	Receiving Sensitivity (Typ.)			3GPP Requirement (SIMO)
	Primary	Diversity	SIMO	
GSM850	-109.3	-	-	-102 dBm
EGSM900	-108.2	-	-	-102 dBm
DCS1800	-106.8	-	-	-102 dBm
PCS1900	-107	-	-	-102 dBm
WCDMA B1	-109.2	-	-	-106.7 dBm
WCDMA B2	-107.7	-	-	-104.7 dBm
WCDMA B4	-109.2	-	-	-106.7 dBm
WCDMA B5	-110.7	-	-	-104.7 dBm
WCDMA B8	-110.2	-	-	-103.7 dBm
LTE-FDD B1	-97.8	-97.8	-101	-96.3 dBm
LTE FDD B2	-96.1	-97.8	-100.2	-94.3 dBm
LTE-FDD B3	-96.7	-97.5	-100.9	-93.3 dBm
LTE FDD B4	--97	-97.4	-101.1	-96.3 dBm
LTE-FDD B5	-98.2	-99.2	-101.7	-94.3 dBm
LTE-FDD B7	-95.8	-97.3	-99.9	-94.3 dBm
LTE-FDD B8	-96.9	-98.6	-100.2	-93.3 dBm
LTE-FDD B28	-98.5	-99.3	-102.4	-94.8 dBm
LTE-FDD B66	-97	-97.7	-100	-96.5 dBm

LTE-TDD B40	-96.9	-98.5	-101.3	-96.3 dBm

Table 36: Conducted RF Receiving Sensitivity of EC200A-EU

Frequency	Receiving Sensitivity (Typ.)			3GPP Requirement (SIMO)
	Primary	Diversity	SIMO	
EGSM900	-108.7	-	-	-102 dBm
DCS1800	-107	-	-	-102 dBm
WCDMA B1	-109.7	-	-	-106.7 dBm
WCDMA B5	-111	-	-	-104.7 dBm
WCDMA B8	-110.5	-	-	-103.7 dBm
LTE-FDD B1	-96.9	-97	-100.8	-96.3 dBm
LTE-FDD B3	-95.9	-96.8	-100.4	-93.3 dBm
LTE-FDD B5	-98.3	-99	-102.2	-94.3 dBm
LTE-FDD B7	-94.4	-95.8	-98	-94.3 dBm
LTE-FDD B8	-96.7	-98.9	-100.1	-93.3 dBm
LTE-FDD B20	-98.1	-99.3	-101.4	-93.3 dBm
LTE-FDD B28	-98.9	-99.5	-102.6	-94.8 dBm
LTE-TDD B38	-96.5	-96.4	-99.3	-96.3 dBm
LTE-TDD B40	-97.3	-97.3	-100.5	-96.3 dBm
LTE-TDD B41	-94.9	-95.1	-97.8	-94.3 dBm

Table 37: Conducted RF Receiving Sensitivity of EC200A-EL

Frequency	Receiving Sensitivity (Typ.)			3GPP Requirement (SIMO)
	Primary	Diversity	SIMO	
WCDMA B1	-109	-	-	-106.7 dBm
WCDMA B5	-109	-	-	-104.7 dBm

WCDMA B8	-108.3	-	-	-103.7 dBm
LTE-FDD B1	-97.3	-98.4	-100.2	-96.3 dBm
LTE-FDD B3	-96.4	-96.4	-99.4	-93.3 dBm
LTE-FDD B5	-96.4	-99.1	-101.95	-94.3 dBm
LTE-FDD B7	-96.06	-96.36	-97.6	-94.3 dBm
LTE-FDD B8	-97.4	-98.2	-102.05	-93.3 dBm
LTE-FDD B20	-96.2	-97.50	-100.75	-93.3 dBm
LTE-FDD B28	-96.7	-97.9	-97.55	-94.8 dBm
LTE-TDD B38	-98.26	-97	-99.3	-96.3 dBm
LTE-TDD B40	-98.46	-97.96	-99.2	-96.3 dBm
LTE-TDD B41	-98.4	-95.4	-99.1	-94.3 dBm

5.1.4. Reference Design

The module provides two RF antenna interfaces for antenna connection.

It is recommended to reserve a π-type matching circuit for better RF performance, and the π-type matching components (C1, R1, C2 and C3, R2, C4) should be placed as close to the antenna as possible. The capacitors are not mounted by default.

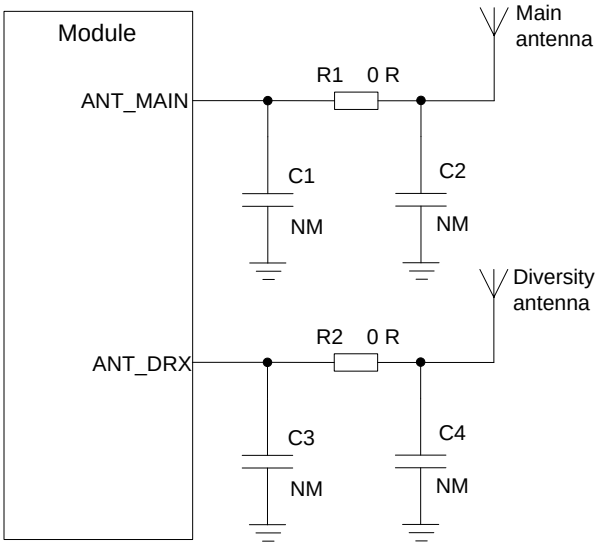


Figure 33: Reference Circuit for RF Antenna Interfaces

5.2. Reference Design of RF Routing

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

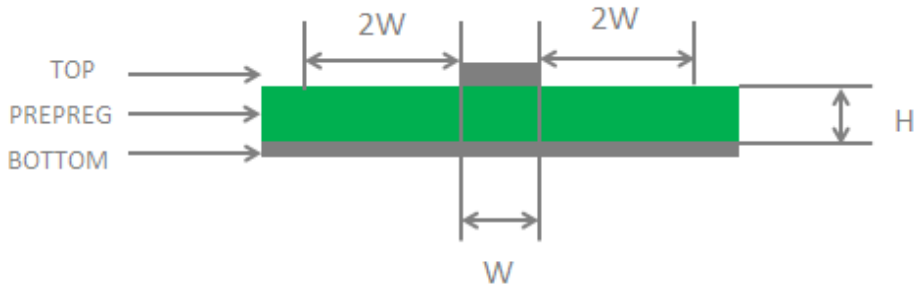


Figure 34: Microstrip Design on a 2-layer PCB

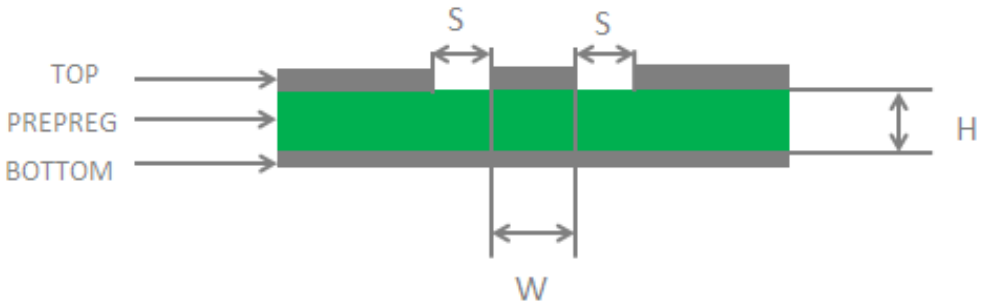


Figure 35: Coplanar Waveguide Design on a 2-layer PCB

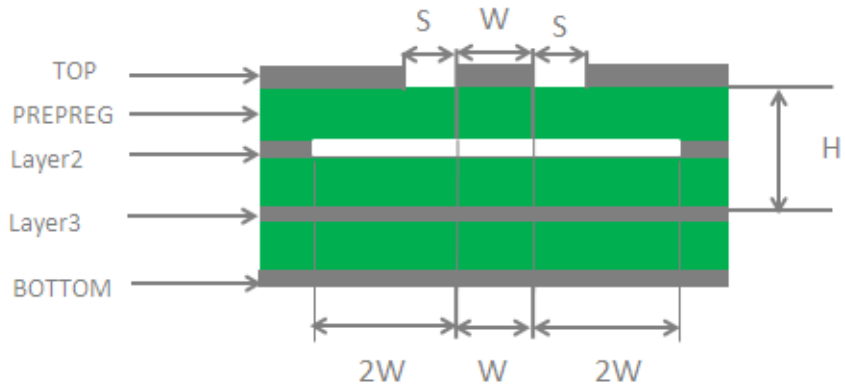


Figure 36: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

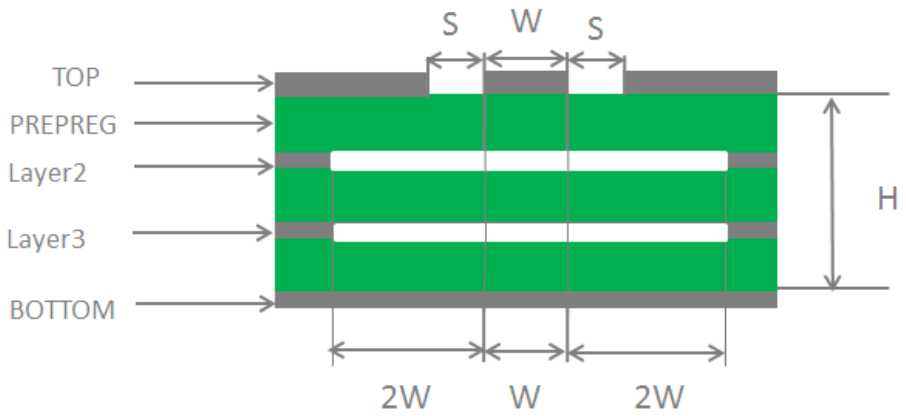


Figure 37: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, ground vias around RF traces and the reference ground improves RF performance. The distance between the ground vias and RF traces should be more than two times the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, please refer to ***document [3]***.

5.3. Requirements for Antenna Design

Table 38: Requirements for Antenna Design

Antenna Type	Requirements
GSM/UMTS/LTE	VSWR: ≤ 2 Efficiency: > 30 % Gain: 1dBi Max. input power: 50 W Input impedance: 50 Ω Cable insertion loss: **< 1 dB**：LB（< 1 GHz） **< 1.5 dB**：MB（1–2.3 GHz） **< 2 dB**：HB（> 2.3 GHz）

5.4. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connector provided by Hirose.

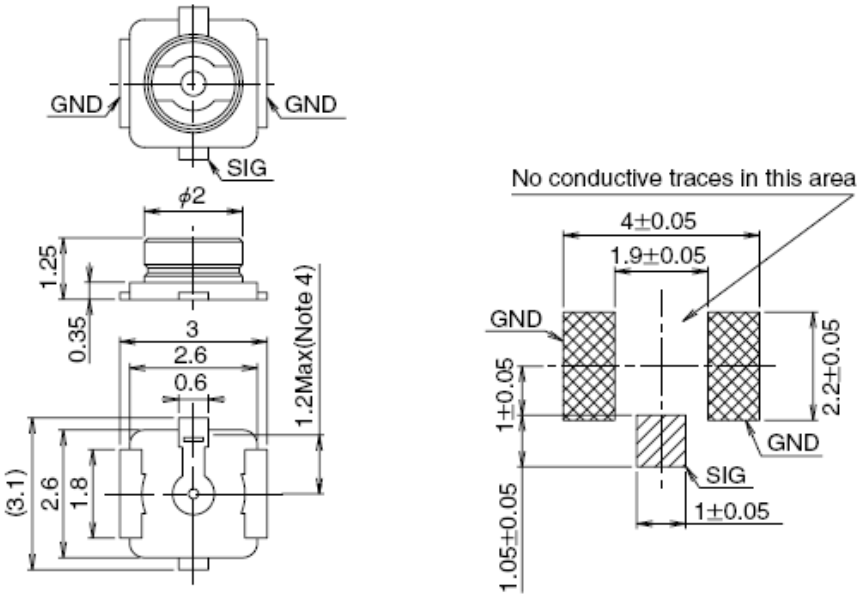


Figure 38: Dimensions of the Receptacle (Unit: mm)

U.FL-LP serial mated plugs listed in the following figure can be used to match the U.FL-R-SMT connector.

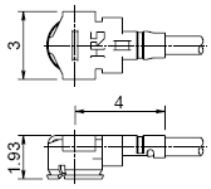
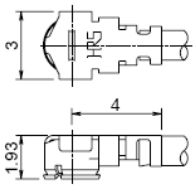
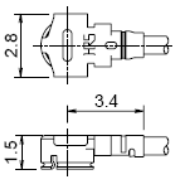
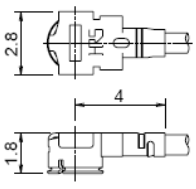
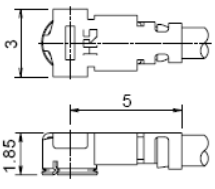
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 39: Specifications of Mated Plugs

The following figure describes the space factor of mated connector.

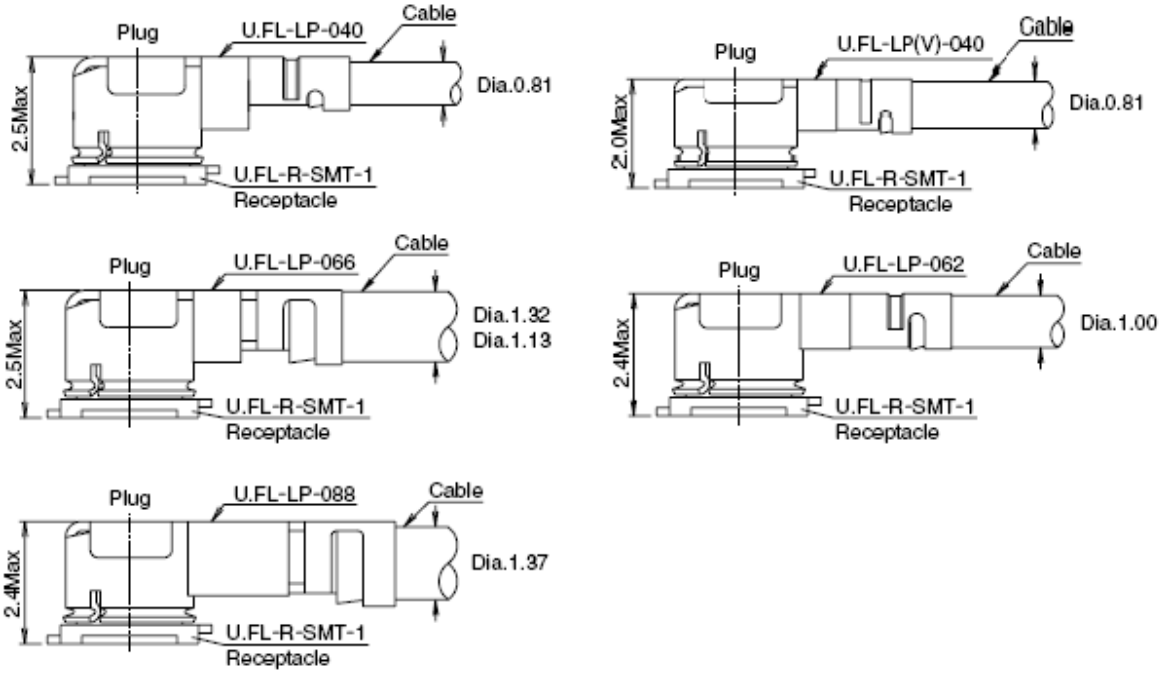


Figure 40: Space Factor of Mated Connector (Unit: mm)

For more details, please visit http://hirose.com.

6 Electrical Characteristics & Reliability

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 39: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	5.5	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	-	0.8	A
Peak Current of VBAT_RF	-	2.0	A
Voltage on Digital Pins	-0.3	2.3	V
Voltage at ADC0	0	VBAT_BB	V
Voltage at ADC1	0	VBAT_BB	V

6.2. Power Supply Ratings

Table 40: The Module's Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must stay between the minimum and maximum values.	3.4	3.8	4.5	V
	Voltage drop during transmitting burst	Maximum power control level at EGSM 900	0	0	400	mV
I_{VBAT_RF}	Peak supply current (during transmission slot)	Maximum power control level at EGSM 900	-	-	2.0	A
USB_VBUS	USB connection detection		3.0	5.0	5.25	V

6.3. Power Consumption

Table 41: EC200A-CN Current Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	12	uA
Sleep state	**AT+CFUN=0** (USB disconnected)	0.91	mA
	EGSM900 @ DRX = 2 (USB disconnected)	1.74	mA
	EGSM900 @ DRX = 5 (USB disconnected)	1.31	mA
	EGSM900 @ DRX = 5 (USB suspend)	1.46	mA
	EGSM900 @ DRX = 9 (USB disconnected)	1.18	mA
	DCS1800 @ DRX = 2 (USB disconnected)	1.74	mA
	DCS1800 @ DRX = 5 (USB disconnected)	1.31	mA
	DCS1800 @ DRX = 5 (USB suspend)	1.45	mA

	DCS1800 @ DRX = 9 (USB disconnected)	1.17	mA
	WCDMA @ PF = 64 (USB disconnected)	2.40	mA
	WCDMA @ PF = 64 (USB suspend)	2.57	mA
	WCDMA @ PF = 128 (USB disconnected)	1.70	mA
	WCDMA @ PF = 256 (USB disconnected)	1.35	mA
	WCDMA @ PF = 512 (USB disconnected)	1.19	mA
	LTE-FDD @ PF = 32 (USB disconnected)	2.06	mA
	LTE-FDD @ PF = 64 (USB disconnected)	1.46	mA
	LTE-FDD @ PF = 64 (USB suspend)	1.62	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.20	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.07	mA
	LTE-TDD @ PF = 32 (USB disconnected)	2.05	mA
	LTE-TDD @ PF = 64 (USB disconnected)	1.47	mA
	LTE-TDD @ PF = 64 (USB suspend)	1.62	mA
	LTE-TDD @ PF = 128 (USB disconnected)	1.20	mA
	LTE-TDD @ PF = 256 (USB disconnected)	1.07	mA
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	19.51	mA
	EGSM900 @ DRX = 5 (USB connected)	34.16	mA
	WCDMA @ PF = 64 (USB disconnected)	20.17	mA
	WCDMA @ PF = 64 (USB connected)	34.79	mA
	LTE-FDD @ PF = 64 (USB disconnected)	20.03	mA
	LTE-FDD @ PF = 64 (USB connected)	34.70	mA
	LTE-TDD @ PF = 64 (USB disconnected)	19.90	mA
	LTE-TDD @ PF = 64 (USB connected)	34.72	mA
GPRS data transfer	EGSM900 4DL/1UL @ 32.34 dBm	197.6	mA

	EGSM900 3DL/2UL @ 32.31 dBm	364.8	mA
	EGSM900 2DL/3UL @ 31.08 dBm	468.8	mA
	EGSM900 1DL/4UL @ 29.28 dBm	523.2	mA
	DCS1800 4DL/1UL @ 29.65 dBm	134.3	mA
	DCS1800 3DL/2UL @ 29.58 dBm	242.3	mA
	DCS1800 2DL/3UL @ 28.03 dBm	281.8	mA
	DCS1800 1DL/4UL @ 26.16 dBm	298.5	mA
EDGE data transfer	EGSM900 4DL/1UL @ 27.06 dBm	136.6	mA
	EGSM900 3DL/2UL @ 26.87 dBm	243.3	mA
	EGSM900 2DL/3UL @ 25.01 dBm	314.2	mA
	EGSM900 1DL/4UL @ 22.87 dBm	359.2	mA
	DCS1800 4DL/1UL @ 25.66 dBm	119.4	mA
	DCS1800 3DL/2UL @ 25.50 dBm	214.1	mA
	DCS1800 2DL/3UL @ 23.95 dBm	289.1	mA
	DCS1800 1DL/4UL @ 21.93 dBm	344.8	mA
WCDMA data transfer	WCDMA B1 HSDPA @ 22.06 dBm	511.97	mA
	WCDMA B5 HSDPA @ 21.68 dBm	443.02	mA
	WCDMA B8 HSDPA @ 21.64 dBm	483.22	mA
	WCDMA B1 HSUPA @ 21.30 dBm	489.72	mA
	WCDMA B5 HSUPA @ 20.02 dBm	405.29	mA
	WCDMA B8 HSUPA @ 21.03 dBm	451.78	mA
LTE data transfer	LTE-FDD B1 @ 22.78 dBm	563.82	mA
	LTE-FDD B3 @ 23.39 dBm	583.24	mA
	LTE-FDD B5 @ 23.19 dBm	530.15	mA
	LTE-FDD B8 @ 23.87 dBm	578.26	mA

	LTE-TDD B34 @ 22.83 dBm	228.47	mA
	LTE-TDD B38 @ 23.55 dBm	357.07	mA
	LTE-TDD B39 @ 23.09 dBm	236.27	mA
	LTE-TDD B40 @ 23.19 dBm	333.39	mA
	LTE-TDD B41 @ 23.44 dBm	381.70	mA
GSM voice call	EGSM900 PCL = 5 @ 32.24 dBm	202.3	mA
	EGSM900 PCL = 12 @ 19.09 dBm	74.5	mA
	EGSM900 PCL = 19 @ 5.82 dBm	47.2	mA
	DCS1800 PCL = 0 @ 29.40 dBm	134.9	mA
	DCS1800 PCL = 7 @ 15.75 dBm	59.4	mA
	DCS1800 PCL = 15 @ -0.43 dBm	46.8	mA
WCDMA voice call	WCDMA B1 @ 22.77 dBm	557.69	mA
	WCDMA B5 @ 22.42 dBm	483.34	mA
	WCDMA B8 @ 22.43 dBm	529.50	mA

Table 42: EC200A-AU Current Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	12	uA
Sleep state	**AT+CFUN=0** (USB disconnected)	0.84	mA
	EGSM900 @ DRX = 2 (USB disconnected)	1.77	mA
	EGSM900 @ DRX = 5 (USB disconnected)	1.22	mA
	EGSM900 @ DRX = 5 (USB suspend)	1.46	mA
	EGSM900 @ DRX = 9 (USB disconnected)	1.10	mA
	DCS1800 @ DRX = 2 (USB disconnected)	1.78	mA
	DCS1800 @ DRX = 5 (USB disconnected)	1.23	mA

	DCS1800 @ DRX = 5 (USB suspend)	1.35	mA
	DCS1800 @ DRX = 9 (USB disconnected)	1.13	mA
	WCDMA @ PF = 64 (USB disconnected)	2.28	mA
	WCDMA @ PF = 64 (USB suspend)	2.48	mA
	WCDMA @ PF = 128 (USB disconnected)	1.63	mA
	WCDMA @ PF = 256 (USB disconnected)	1.29	mA
	WCDMA @ PF = 512 (USB disconnected)	1.13	mA
	LTE-FDD @ PF = 32 (USB disconnected)	2.02	mA
	LTE-FDD @ PF = 64 (USB disconnected)	1.46	mA
	LTE-FDD @ PF = 64 (USB suspend)	1.62	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.18	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.05	mA
	LTE-TDD @ PF = 32 (USB disconnected)	2.04	mA
	LTE-TDD @ PF = 64 (USB disconnected)	1.45	mA
	LTE-TDD @ PF = 64 (USB suspend)	1.61	mA
	LTE-TDD @ PF = 128 (USB disconnected)	1.19	mA
	LTE-TDD @ PF = 256 (USB disconnected)	1.06	mA
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	18.30	mA
	EGSM900 @ DRX = 5 (USB connected)	32.78	mA
	WCDMA @ PF = 64 (USB disconnected)	18.91	mA
	WCDMA @ PF = 64 (USB connected)	33.35	mA
	LTE-FDD @ PF = 64 (USB disconnected)	18.60	mA
	LTE-FDD @ PF = 64 (USB connected)	33.17	mA
	LTE-TDD @ PF = 64 (USB disconnected)	18.64	mA
	LTE-TDD @ PF = 64 (USB connected)	33.18	mA

GPRS data transfer	GSM850 4DL/1UL @ 31.77 dBm	231	mA
	GSM850 3DL/2UL @ 31.79 dBm	389	mA
	GSM850 2DL/3UL @ 30.80 dBm	497	mA
	GSM850 1DL/4UL @ 29.19 dBm	548	mA
	EGSM900 4DL/1UL @ 31.61 dBm	189	mA
	EGSM900 3DL/2UL @ 31.59 dBm	357	mA
	EGSM900 2DL/3UL @ 30.58 dBm	466	mA
	EGSM900 1DL/4UL @ 28.99 dBm	522	mA
	DCS1800 4DL/1UL @ 28.53 dBm	144	mA
	DCS1800 3DL/2UL @ 28.42 dBm	270	mA
	DCS1800 2DL/3UL @ 27.54 dBm	331	mA
	DCS1800 1DL/4UL @ 25.85 dBm	351	mA
	PCS1900 4DL/1UL @ 27.61 dBm	218	mA
	PCS1900 3DL/2UL @ 27.33 dBm	361	mA
	PCS1900 2DL/3UL @ 27.17 dBm	435	mA
	PCS1900 1DL/4UL @ 26.20 dBm	427	mA
EDGE data transfer	GSM850 4DL/1UL @ 26.38 dBm	133	mA
	GSM850 3DL/2UL @ 24.64 dBm	217	mA
	GSM850 2DL/3UL @ 22.53 dBm	283	mA
	GSM850 1DL/4UL @ 20.50 dBm	350	mA
	EGSM900 4DL/1UL @ 26.74 dBm	136	mA
	EGSM900 3DL/2UL @ 24.71 dBm	223	mA
	EGSM900 2DL/3UL @ 22.57 dBm	288	mA
	EGSM900 1DL/4UL @ 20.29 dBm	351	mA
	DCS1800 4DL/1UL @ 25.81 dBm	122	mA

	DCS1800 3DL/2UL @ 24.29 dBm	211	mA
	DCS1800 2DL/3UL @ 22.24 dBm	282	mA
	DCS1800 1DL/4UL @ 19.89 dBm	354	mA
	PCS1900 4DL/1UL @ 25.93 dBm	121	mA
	PCS1900 3DL/2UL @ 24.34 dBm	207	mA
	PCS1900 2DL/3UL @ 22.31 dBm	280	mA
	PCS1900 1DL/4UL @ 20.09 dBm	354	mA
WCDMA data transfer	WCDMA B1 HSDPA @ 21.98 dBm	530	mA
	WCDMA B2 HSDPA @ 21.78 dBm	547	mA
	WCDMA B4 HSDPA @ 21.96 dBm	552	mA
	WCDMA B5 HSDPA @ 21.70 dBm	501	mA
	WCDMA B8 HSDPA @ 21.64 dBm	534	mA
	WCDMA B1 HSUPA @ 21.99 dBm	484	mA
	WCDMA B2 HSUPA @ 21.61 dBm	535	mA
	WCDMA B4 HSUPA @ 20.68 dBm	501	mA
	WCDMA B5 HSUPA @ 21.42 dBm	481	mA
	WCDMA B8 HSUPA @ 21.45 dBm	523	mA
LTE data transfer	LTE-FDD B1 @ 22.76 dBm	553.4	mA
	LTE-FDD B2 @ 23.06 dBm	501.64	mA
	LTE-FDD B3 @ 22.32 dBm	515.51	mA
	LTE-FDD B4 @ 23.31 dBm	470.45	mA
	LTE-FDD B5 @ 22.73 dBm	439.9	mA
	LTE-FDD B7 @ 23.04 dBm	618.68	mA
	LTE-FDD B8 @ 23.39 dBm	470.43	mA
	LTE-FDD B28A @ 23.33 dBm	441.96	mA

	LTE-FDD B28B @ 22.44 dBm	436.96	mA
	LTE-FDD B66 @ 23.59 dBm	510.83	mA
	LTE-TDD B40 @ 22.64 dBm	228.16	mA
GSM voice call	EGSM900 PCL = 5 @ 31.55 dBm	234	mA
	EGSM900 PCL = 12 @ 18.87 dBm	111	mA
	EGSM900 PCL = 19 @ 5.58 dBm	81	mA
	DCS1800 PCL = 0 @ 28.50 dBm	183	mA
	DCS1800 PCL = 7 @ 15.62 dBm	97	mA
	DCS1800 PCL = 15 @ 0.32 dBm	77	mA
WCDMA voice call	WCDMA B1 @ 23.08 dBm	587	mA
	WCDMA B2 @ 22.72 dBm	602	mA
	WCDMA B4 @ 23.28 dBm	602	mA
	WCDMA B5 @ 22.69 dBm	552	mA
	WCDMA B8 @ 22.61 dBm	593	mA

Table 43: EC200A-EU Current Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	11	uA
Sleep state	**AT+CFUN=0** (USB disconnected)	0.94	mA
	EGSM900 @ DRX = 2 (USB disconnected)	1.67	mA
	EGSM900 @ DRX = 5 (USB disconnected)	1.24	mA
	EGSM900 @ DRX = 5 (USB suspend)	1.40	mA
	EGSM900 @ DRX = 9 (USB disconnected)	1.09	mA
	DCS1800 @ DRX = 2 (USB disconnected)	1.68	mA
	DCS1800 @ DRX = 5 (USB disconnected)	1.26	mA

	DCS1800 @ DRX = 5 (USB suspend)	1.39	mA
	DCS1800 @ DRX = 9 (USB disconnected)	1.14	mA
	WCDMA @ PF = 64 (USB disconnected)	2.26	mA
	WCDMA @ PF = 64 (USB suspend)	2.41	mA
	WCDMA @ PF = 128 (USB disconnected)	1.59	mA
	WCDMA @ PF = 256 (USB disconnected)	1.25	mA
	WCDMA @ PF = 512 (USB disconnected)	1.07	mA
	LTE-FDD @ PF = 32 (USB disconnected)	1.98	mA
	LTE-FDD @ PF = 64 (USB disconnected)	1.41	mA
	LTE-FDD @ PF = 64 (USB suspend)	1.55	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.15	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.02	mA
	LTE-TDD @ PF = 32 (USB disconnected)	2.02	mA
	LTE-TDD @ PF = 64 (USB disconnected)	1.42	mA
	LTE-TDD @ PF = 64 (USB suspend)	1.58	mA
	LTE-TDD @ PF = 128 (USB disconnected)	1.16	mA
	LTE-TDD @ PF = 256 (USB disconnected)	1.02	mA
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	18.27	mA
	EGSM900 @ DRX = 5 (USB connected)	32.85	mA
	WCDMA @ PF = 64 (USB disconnected)	18.89	mA
	WCDMA @ PF = 64 (USB connected)	33.43	mA
	LTE-FDD @ PF = 64 (USB disconnected)	18.45	mA
	LTE-FDD @ PF = 64 (USB connected)	32.99	mA
	LTE-TDD @ PF = 64 (USB disconnected)	18.44	mA
	LTE-TDD @ PF = 64 (USB connected)	33.02	mA

GPRS data transfer	EGSM900 4DL/1UL @ 32.44 dBm	199	mA
	EGSM900 3DL/2UL @ 32.39 dBm	372	mA
	EGSM900 2DL/3UL @ 31.23 dBm	478	mA
	EGSM900 1DL/4UL @ 29.53 dBm	533	mA
	DCS1800 4DL/1UL @ 29.77 dBm	136	mA
	DCS1800 3DL/2UL @ 29.65 dBm	244	mA
	DCS1800 2DL/3UL @ 28.31 dBm	293	mA
	DCS1800 1DL/4UL @ 26.40 dBm	309	mA
EDGE data transfer	EGSM900 4DL/1UL @ 27.01 dBm	137	mA
	EGSM900 3DL/2UL @ 26.98 dBm	246	mA
	EGSM900 2DL/3UL @ 25.27 dBm	315	mA
	EGSM900 1DL/4UL @ 23.13 dBm	375	mA
	DCS1800 4DL/1UL @ 25.96 dBm	121	mA
	DCS1800 3DL/2UL @ 25.77 dBm	215	mA
	DCS1800 2DL/3UL @ 24.24 dBm	289	mA
	DCS1800 1DL/4UL @ 22.10 dBm	360	mA
WCDMA data transfer	WCDMA B1 HSDPA @ 21.99 dBm	520	mA
	WCDMA B5 HSDPA @ 21.76 dBm	474	mA
	WCDMA B8 HSDPA @ 21.81 dBm	496	mA
	WCDMA B1 HSUPA @ 21.21 dBm	504	mA
	WCDMA B5 HSUPA @ 21.13 dBm	454	mA
	WCDMA B8 HSUPA @ 21.49 dBm	497	mA
LTE data transfer	LTE-FDD B1 @ 23.61 dBm	607	mA
	LTE-FDD B3 @ 23.71 dBm	636	mA
	LTE-FDD B5 @ 23.70 dBm	568	mA

	LTE-FDD B7 @ 23.56 dBm	813	mA
	LTE-FDD B8 @ 24.11 dBm	591	mA
	LTE-FDD B20 @ 23.20 dBm	592	mA
	LTE-FDD B28 @ 23.77 dBm	559	mA
	LTE-TDD B38 @ 18.12 dBm	230	mA
	LTE-TDD B40 @ 18.68 dBm	233	mA
	LTE-TDD B41 @ 19.18 dBm	242	mA
GSM voice call	EGSM900 PCL = 5 @ 32.34 dBm	206	mA
	EGSM900 PCL = 12 @ 19.11 dBm	76	mA
	EGSM900 PCL = 19 @ 6.05 dBm	48	mA
	DCS1800 PCL = 0 @ 29.50 dBm	136	mA
	DCS1800 PCL = 7 @ 16.07 dBm	61	mA
	DCS1800 PCL = 15 @ -1.14 dBm	48	mA
WCDMA voice call	WCDMA B1 @ 22.29 dBm	543	mA
	WCDMA B5 @ 22.26 dBm	496	mA
	WCDMA B8 @ 22.25 dBm	533	mA

Table 44: EC200A-EL Current Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	16	uA
Sleep state	**AT+CFUN=0** (USB disconnected)	0.73	mA
	WCDMA @ PF = 64 (USB disconnected)	2.26	mA
	WCDMA @ PF = 64 (USB suspend)	2.39	mA
	WCDMA @ PF = 128 (USB disconnected)	1.56	mA
	WCDMA @ PF = 256 (USB disconnected)	1.19	mA

	WCDMA @ PF = 512 (USB disconnected)	1.04	mA
	LTE-FDD @ PF = 32 (USB disconnected)	1.92	mA
	LTE-FDD @ PF = 64 (USB disconnected)	1.35	mA
	LTE-FDD @ PF = 64 (USB suspend)	1.52	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.08	mA
	LTE-FDD @ PF = 256 (USB disconnected)	0.94	mA
	LTE-TDD @ PF = 32 (USB disconnected)	1.97	mA
	LTE-TDD @ PF = 64 (USB disconnected)	1.37	mA
	LTE-TDD @ PF = 64 (USB suspend)	1.53	mA
	LTE-TDD @ PF = 128 (USB disconnected)	1.12	mA
	LTE-TDD @ PF = 256 (USB disconnected)	0.96	mA
Idle state	WCDMA @ PF = 64 (USB disconnected)	20.29	mA
	WCDMA @ PF = 64 (USB connected)	34.78	mA
	LTE-FDD @ PF = 64 (USB disconnected)	19.77	mA
	LTE-FDD @ PF = 64 (USB connected)	34.27	mA
	LTE-TDD @ PF = 64 (USB disconnected)	19.82	mA
	LTE-TDD @ PF = 64 (USB connected)	34.33	mA
WCDMA data transfer	WCDMA B1 HSDPA @ 21.73 dBm	560	mA
	WCDMA B5 HSDPA @ 21.92 dBm	466	mA
	WCDMA B8 HSDPA @ 22.06 dBm	525	mA
	WCDMA B1 HSUPA @ 21.03 dBm	532	mA
	WCDMA B5 HSUPA @21.36 dBm	448	mA
	WCDMA B8 HSUPA @ 21.41 dBm	483	mA
LTE data transfer	LTE-FDD B1 @ 22.88 dBm	627	mA
	LTE-FDD B3 @ 23.76 dBm	611	mA

	LTE-FDD B5 @ 23.68 dBm	531	mA
	LTE-FDD B7 @ 23.56 dBm	TBD	mA
	LTE-FDD B8 @ 23.59 dBm	592	mA
	LTE-FDD B20 @ 23.20 dBm	TBD	mA
	LTE-FDD B28 @ 23.77 dBm	TBD	mA
	LTE-TDD B38 @ 23.63dBm	274	mA
	LTE-TDD B39 @ 23.75dBm	276	mA
	LTE-TDD B40 @ 23.41 dBm	245	mA
	LTE-TDD B41 @ 23.58dBm	280	mA
WCDMA voice call	WCDMA B1 @ 22.32 dBm	607	mA
	WCDMA B5 @ 22.59 dBm	499	mA
	WCDMA B8 @ 22.69 dBm	544	mA

6.4. Digital I/O Characteristic

Table 45: 1.8 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
VDD_EXT	Power supply	1.67	1.93	V
VIH	Input high voltage	0.7 × VDD_EXT	VDD_EXT + 0.2	V
VIL	Input low voltage	-0.3	0.3 × VDD_EXT	V
VOH	Output high voltage	VDD_EXT - 0.2	VDD_EXT	V
VOL	Output low voltage	0	0.2	V

Table 46: (U)SIM Low-voltage I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	1.67	1.93	V
V_{IH}	Input high voltage	0.8 × USIM_VDD	USIM_VDD	V
V_{IL}	Input low voltage	-0.3	0.12 × USIM_VDD	V
V_{OH}	Output high voltage	0.7 × USIM_VDD	USIM_VDD	V
V_{OL}	Output low voltage	0	0.15 × USIM_VDD	V

Table 47: (U)SIM High-voltage I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	2.7	3.3	V
V_{IH}	Input high voltage	0.8 × USIM_VDD	USIM_VDD	V
V_{IL}	Input low voltage	-0.3	0.12 × USIM_VDD	V
V_{OH}	Output high voltage	0.7 × USIM_VDD	USIM_VDD	V
V_{OL}	Output low voltage	0	0.15 × USIM_VDD	V

Table 48: SDIO Low-voltage I/O Requirements

Parameter	Description	Min.	Max.	Unit
SD_SDIO_VDD	Power supply	1.67	1.93	V
V_{IH}	Input high voltage	0.7 × SD_SDIO_VDD	SD_SDIO_VDD + 0.2	V
V_{IL}	Input low voltage	-0.3	0.3 × SDIO_VDD	V
V_{OH}	Output high voltage	SDIO_VDD - 0.2	SD_SDIO_VDD	V
V_{OL}	Output low voltage	0	0.2	V

Table 49: SDIO High-voltage I/O Requirements

Parameter	Description	Min.	Max.	Unit
SD_SDIO_VDD	Power supply	2.7	3.05	V
V_{IH}	Input high voltage	2.0	SD_SDIO_VDD + 0.3	V
V_{IL}	Input low voltage	-0.3	0.8	V
V_{OH}	Output high voltage	2.4	SD_SDIO_VDD	V
V_{OL}	Output low voltage	0	0.4	V

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 50: Electrostatics Discharge Characteristics (25 °C, 45 % Relative Humidity)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±8	±10	kV
All Antenna Interfaces	±8	±10	kV
Other Interfaces	±0.5	±1	kV

6.6. Operating and Storage Temperatures

Table 51: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [3]	-35	+25	+75	°C
Extended Operating Temperature Range [4]	-40	-	+85	°C
Storage temperature range	-40	-	+95	°C

[3] Within operating temperature range, the module is 3GPP compliant.
[4] Within the extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as Pout, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

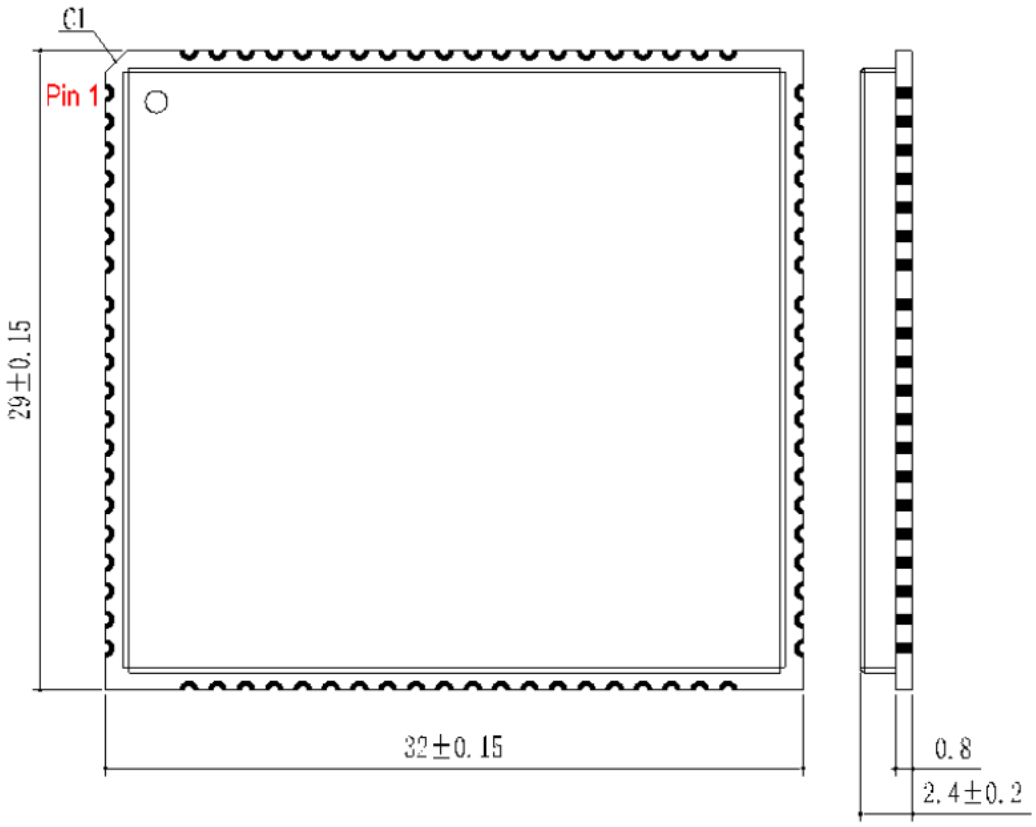


Figure 41: Module Top and Side Dimensions (Unit: mm)

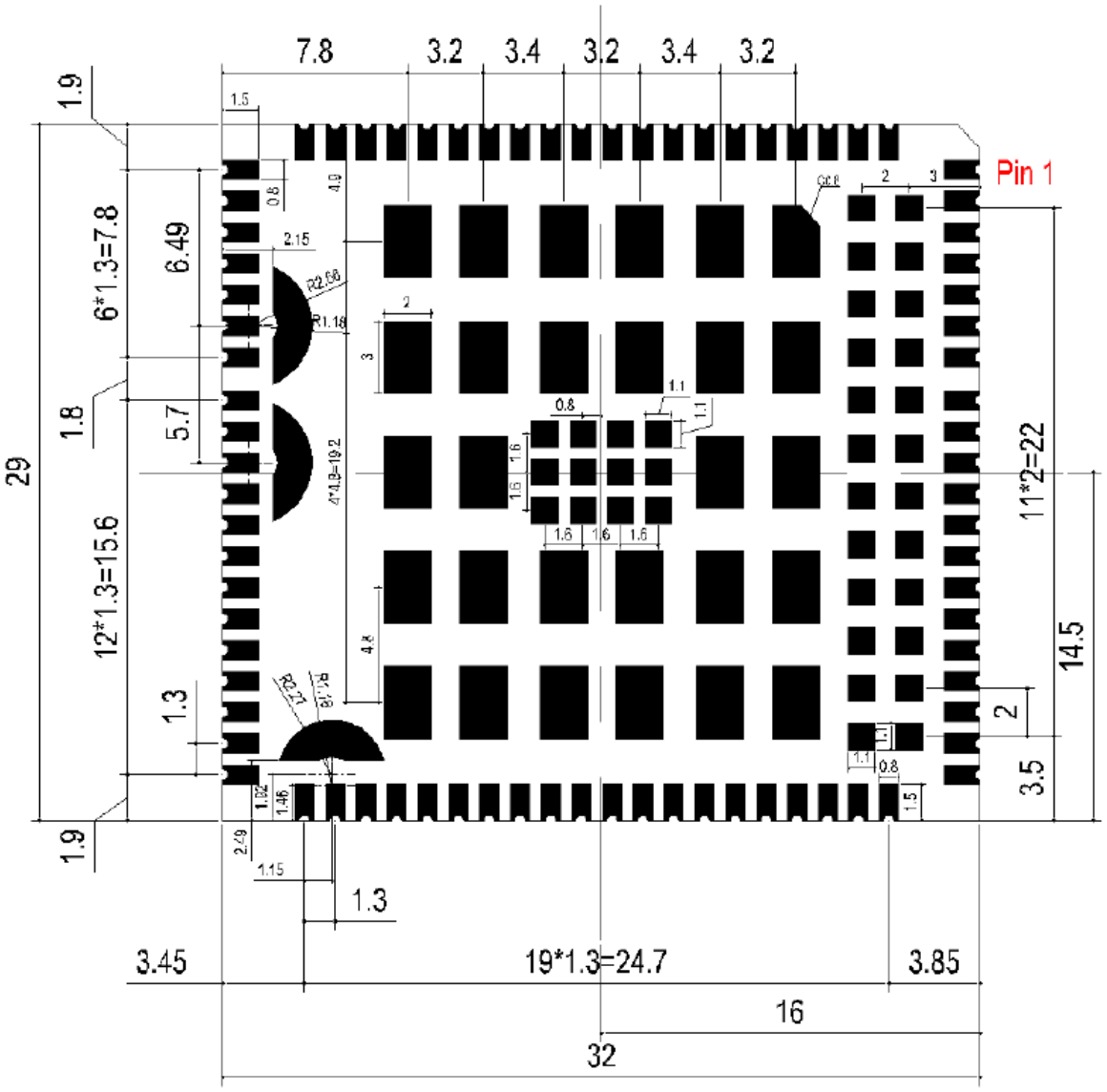


Figure 42: Module Bottom Dimensions View (Unit: mm)

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

7.2. Recommended Footprint

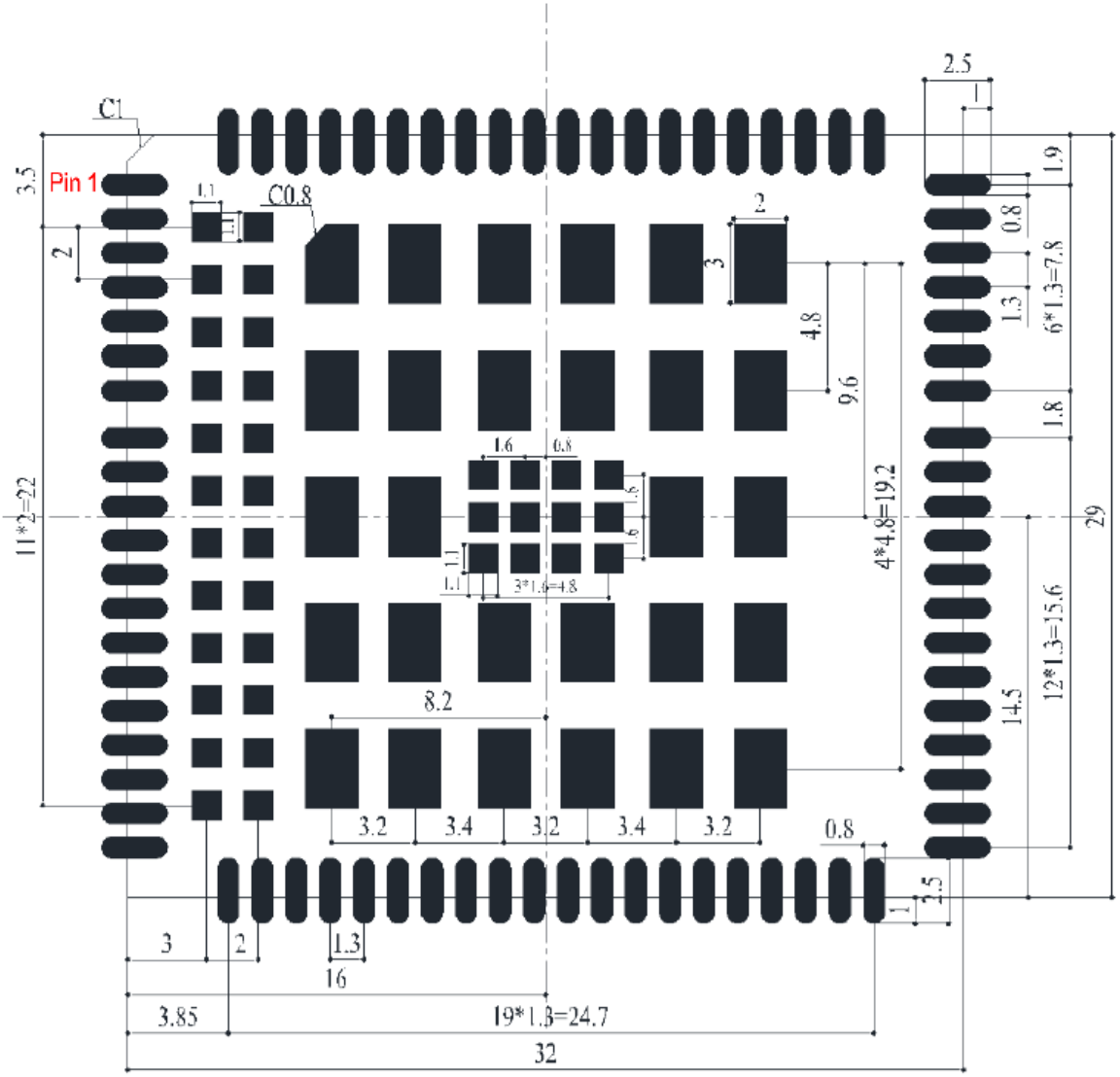


Figure 43: Recommended Footprint (Perspective View)

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

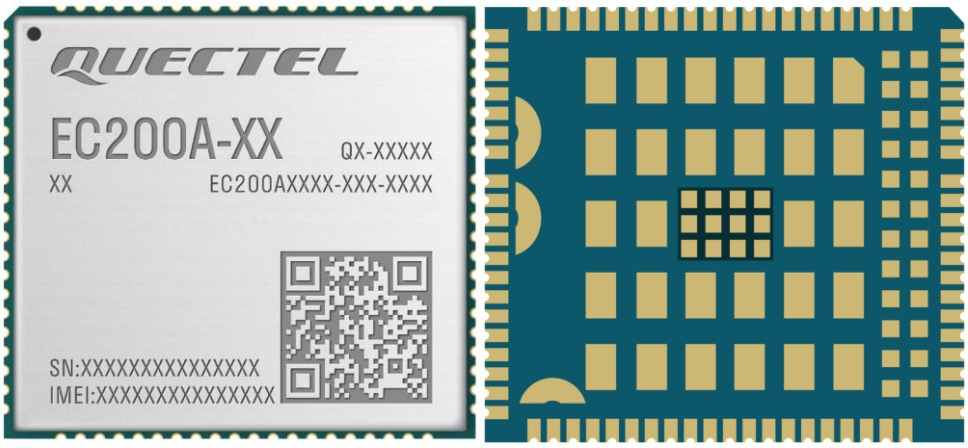


Figure 44: Top and Bottom Views of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed package. MSL of the module is rated as 3, and its storage restrictions are shown as below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. The storage life (in vacuum-sealed packaging) is 12 months in Recommended Storage Condition.

3. The floor life of the module is 168 hours [5] in a plant where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 24 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g. a drying cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement above occurs;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - All modules must be soldered to PCB within 24 hours after the baking, otherwise they should be put in a dry environment such as in a drying oven.

[5] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not remove the packages of tremendous modules if they are not ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. All modules must be soldered to PCB within 24 hours after the baking, otherwise put them in the drying oven. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.18~0.20 mm. For more details, see ***document [4]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below:

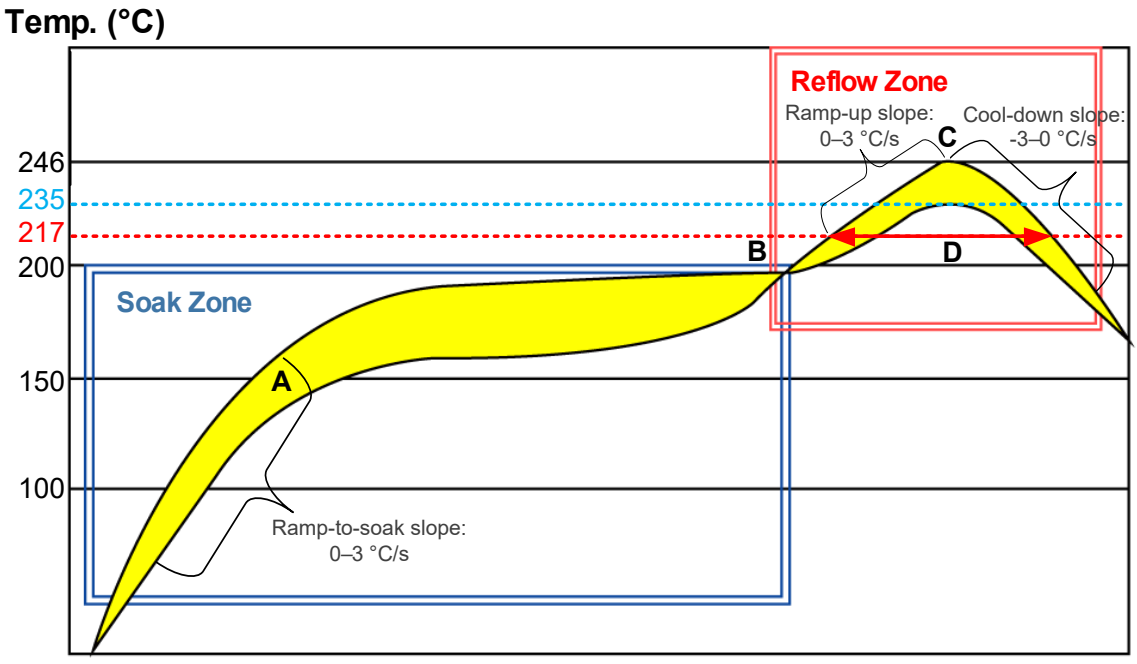


Figure 45: Recommended Reflow Soldering Thermal Profile

Table 52: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217°C)	40–70 s
Max temperature	235–246 °C
Cool-down slope	-3–0 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
3. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6. Due to the complexity of the SMT process, please contact Quectel Technical Supports in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [4]***.

8.3. Packaging Specifications

This chapter describes only the key parameters and process of packaging. All figures below are for reference only. The appearance and structure of the packaging materials are subject to the actual delivery.

The module adopts carrier tape packaging and details are as follow:

8.3.1. Carrier Tape

Dimension details are as follow:

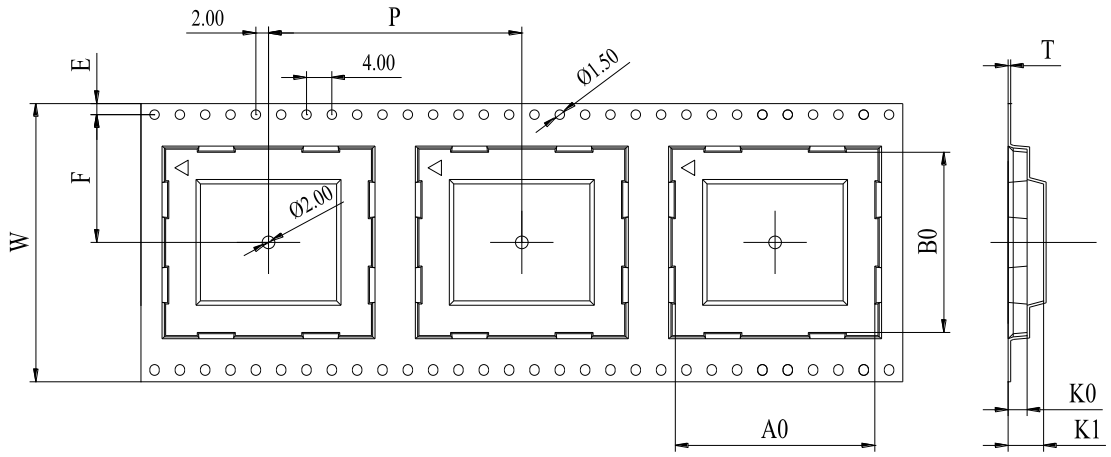


Figure 46: Carrier Tape Dimension Drawing

Table 53: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	44	0.35	32.5	29.5	3.0	3.8	20.2	1.75

8.3.2. Plastic Reel

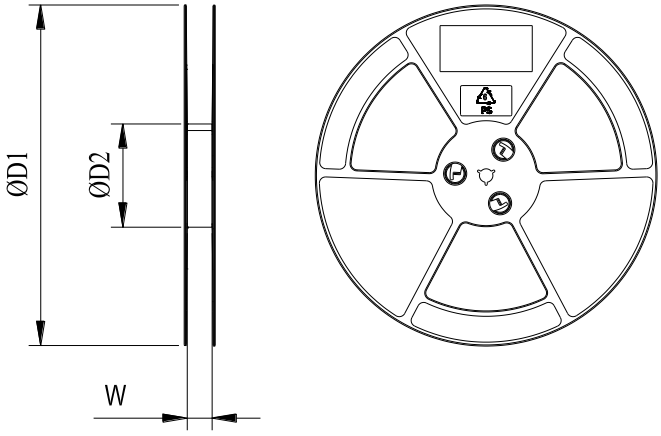
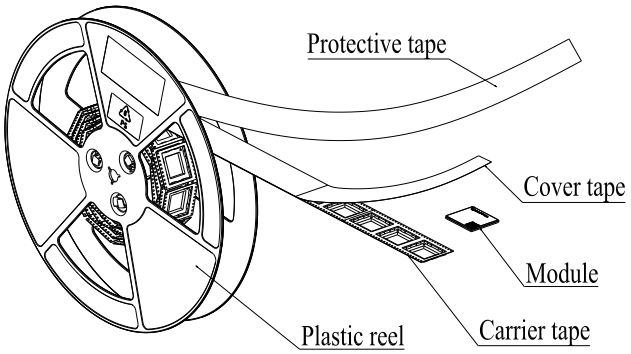


Figure 47: Plastic Reel Dimension Drawing

Table 54: Plastic Reel Dimension Table (Unit: mm)

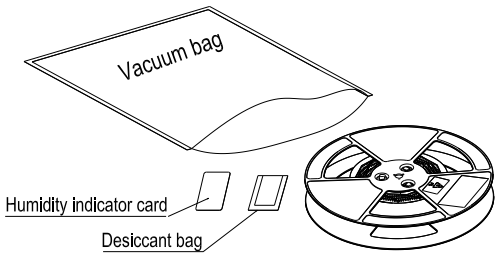
øD1	øD2	W
330	100	44.5

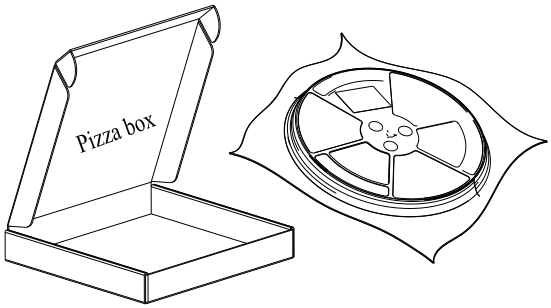
8.3.3. Packaging Process



Place the module into the carrier tape and use the cover tape to cover them; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. One plastic reel can load 250 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, then vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Put 4 pizza boxes into 1 carton and seal it. One carton can pack 1000 modules.

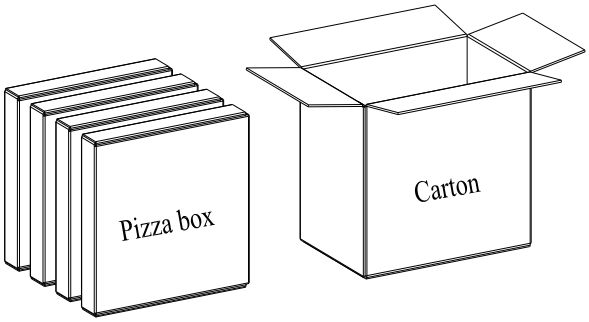


Figure 48: Packaging Process

9 Appendix References

Table 55: Related Documents

Document Name
[1] Quectel_UMTS&LTE_EVB_User_Guide
[2] Quectel_EC200x&EG912Y&EG915N_Series_AT_Commands_Manual
[3] Quectel_RF_Layout_Application_Note
[4] Quectel_Module_SMT_Application_Note

Table 56: Terms and Abbreviations

Abbreviation	Description
AMR	Adaptive Multi-Rate
BeiDou	BeiDou Navigation Satellite System
bps	Bytes per second
CDMA	Code Division Multiple Access
CS	Coding Scheme
CTS	Clear To Send
DRX	Discontinuous Reception
DTE	Data Terminal Equipment
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
ESD	Electrostatic Discharge

EVB	Evaluation Board
FDD	Frequency Division Duplexing
FR	Full Rate
FTP	File Transfer Protocol
FTPS	FTP over SSL
GMSK	Gaussian Filtered Minimum Shift Keying
GND	Ground
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GSM	Global System for Mobile Communications
HR	Half Rate
HSDPA	High Speed Downlink Packet Access
HTTPS	Hypertext Transfer Protocol Secure
LGA	Land Grid Array
LTE	Long Term Evolution
MCS	Modulation and Coding Scheme
MMS	Multimedia Messaging Service
NTP	Network Time Protocol
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PHY	Physical Layer Transceiver
PING	Packet Internet Groper
PPP	Point-to-Point Protocol
PSK	Phase Shift Keying

QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
RTS	Request To Send
SDIO	Secure Digital Input and Output Card
SMS	Short Message Service
SMTP	Simple Mail Transfer Protocol
SMTPS	Simple Mail Transfer Protocol Secure
SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
TDD	Time Division Duplexing
UDP	User Datagram Protocol
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage Value
Vnom	Nominal Voltage Value
Vmin	Minimum Voltage Value
V_{IH}max	Maximum Input High Level Voltage Value
V_{IH}min	Minimum Input High Level Voltage Value
V_{IL}max	Maximum Input Low Level Voltage Value
V_{IL}min	Minimum Input Low Level Voltage Value
V_{OH}min	Minimum Output High Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value

VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access