EC800G-CN
Reference Design

LTE Standard Module Series

Version: 1.1

Date: 2023-01-09

Status: Released

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About the Document

Revision History

Version	Date	Author	Description
-	2022-01-12	Frank WANG /Kyle CHEN	Creation of the document
1.0	2022-07-22	Frank WANG /Kyle CHEN	First official release
1.1	2023-01-09	Frank WANG /Kyle CHEN	1. Updated the description on reserved test points for USB and UART interfaces (Sheets 3 and 10). 2. Updated the reference design of VBAT (Sheet 5). 3. Added the description on reserved test points for RESET and VDD_EXT (Sheet 10).

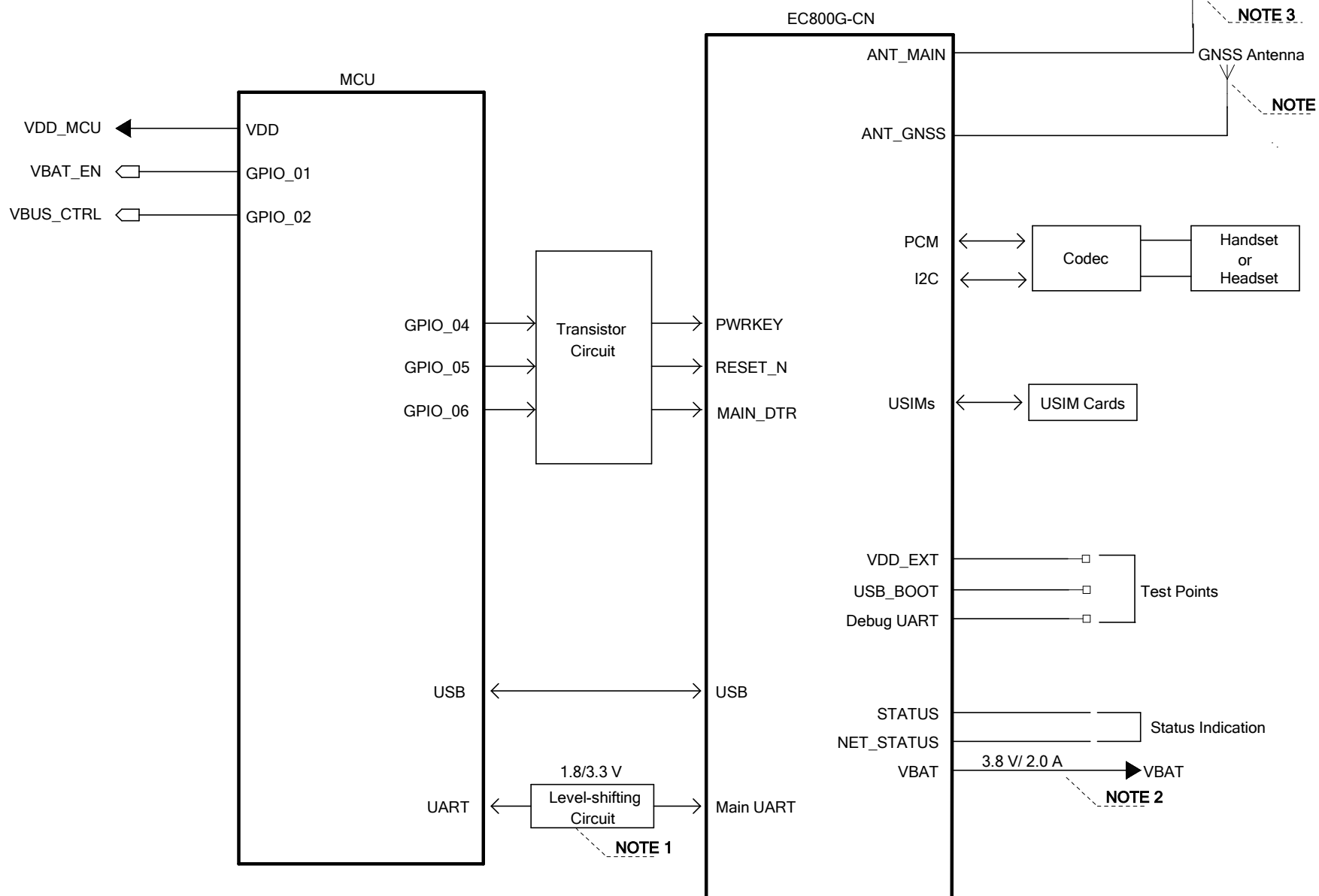# Contents

1 Reference Design

1.1. Introduction

This document provides the reference design for Quectel EC800G-CN module. The reference design mainly includes block diagrams of power supply, UART, USIM and RF interfaces.

1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.
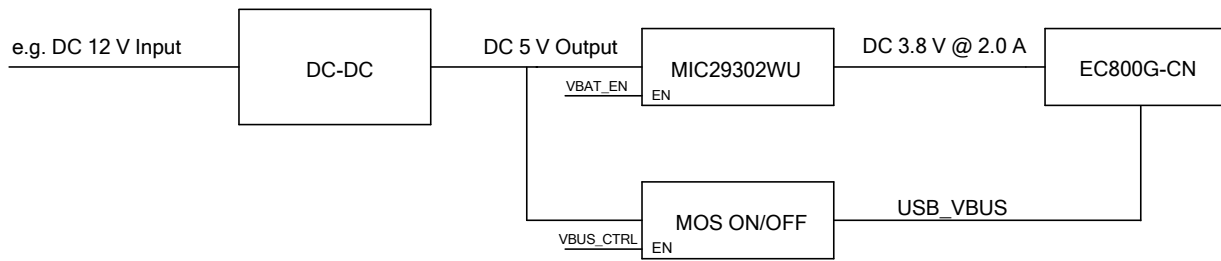
Block Diagram

EC800G-CN

LTE/Wi-Fi Scan Antenna

NOTE 3

ANT_MAIN

GNSS Antenna

NOTE 4

ANT_GNSS

MCU

VDD_MCU ← VDD

VBAT_EN ⊂ GPIO_01

VBUS_CTRL ⊂ GPIO_02

PCM ↔ Codec ↔ Handset or Headset

I2C ↔

GPIO_04 → Transistor Circuit → PWRKEY

GPIO_05 → → RESET_N

GPIO_06 → → MAIN_DTR

USIMs ↔ USIM Cards

VDD_EXT □

USB_BOOT □ Test Points

Debug UART □

USB ↔ USB

STATUS
NET_STATUS — Status Indication

VBAT — 3.8 V/ 2.0 A → VBAT

NOTE 2

1.8/3.3 V

UART ↔ Level-shifting Circuit ↔ Main UART

NOTE 1

NOTE:

1. A level-shifting circuit or a voltage-level translator TXS0108EPWR provided by Texas Instruments is recommended.
2. The power supply should be able to provide sufficient current up to 2.0 A for the module.
3. The module supports Wi-Fi Scan function, which shares the same antenna interface with ANT_MAIN. The two functions cannot be used at the same time.
4. GNSS function is optional for the module.

Power System Block Diagram

```
e.g. DC 12 V Input ──────┤ DC-DC ├──── DC 5 V Output ──┤ MIC29302WU ├── DC 3.8 V @ 2.0 A ──┤ EC800G-CN ├
                                        VBAT_EN ─ EN

                                                        ──┤ MOS ON/OFF ├──── USB_VBUS ──────────────┘
                                        VBUS_CTRL ─ EN
```

Module Interfaces

U0101-C EC800G-CN

Pin	Signal		Signal	Pin
73	GND16		RESERVED44	109
74	RESERVED36		RESERVED45	81
75	RESERVED37		USB_BOOT	82
76	RESERVED38		RESERVED46	83
77	RESERVED39		RESERVED47	84
78	RESERVED40		RESERVED48	85
79	USIM_DET		RESERVED49	86
80	RESERVED41		RESERVED50	87
107	RESERVED42		GND17	88
108	RESERVED43			

USB_BOOT [10]

NOTE 2

[7] USIM_DET

U0101-D EC800G-CN

89	GND18	GND23	94
91	GND19	GND22	92
93	GND20	GND21	90

U0101-A EC800G-CN

VDD-TEST1
VDD-TEST2
VBAT

CODEC

ANT_MAIN [8]
PCM_DOUT [9]
PCM_DIN [9]
PCM_SYNC [9]
PCM_CLK [9]
STATUS [10]
VDD_EXT [5,6,7,9,10]
MAIN_RTS [6]

U0101-B EC800G-CN

I2C_SCL [9]
I2C_SDA [9]
USIM2_VDD
USIM2_DATA [7]
USIM2_RST [7]
USIM2_CLK [7]
USB_VBUS [4,10]
USB_DM_TEST [10]
USB_DP_TEST [10]

NM-0R R0105
NM-0R R0106

L0101 DLM0NSN900HY2D

USB_DM [4]
USB_DP [4]

NOTE 3

NOTE:
1. Keep unused and RESERVED pins open, and connect all GND pins to the ground network.
2. If emergency download is not required, USB_BOOT cannot be pulled down to low level or pulled up to high level and should be kept open before the module is successfully turned on.
3. A common mode choke L0101 is recommended to be added in series between the module and your MCU in order to suppress
   EMI spurious transmission. Meanwhile, test points must be reserved for upgrading firmware and debugging software
   over USB interface and minimize the extra stubs of the trace. L0101 and the two resistors R0105, R0106 should be placed close
   to the module to ensure the integrity of USB signal.
4. Considering the difference of ADC voltage range among Quectel modules, when it is necessary to use ADC pins, it is strongly
   recommended to reserve the voltage divider circuit for better compatibility with other Quectel modules.
   The resistance of the divider must be less than 100 kΩ, otherwise the measurement accuracy of the ADC
   will be significantly reduced. When the divider circuit is not used, the ADC pins require 1 kΩ resistors in series.
5. Circuit wiring design consideration:
   Please ensure that there is a complete reference ground plane below the module, and the ground plane is
   as close to the module layer as possible. It is recommended to design at least 4 layers.

Quectel Wireless Solutions

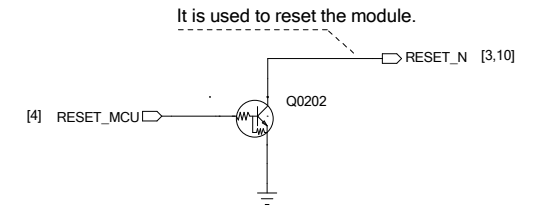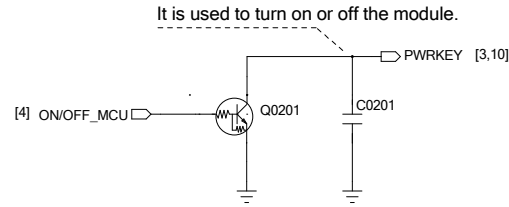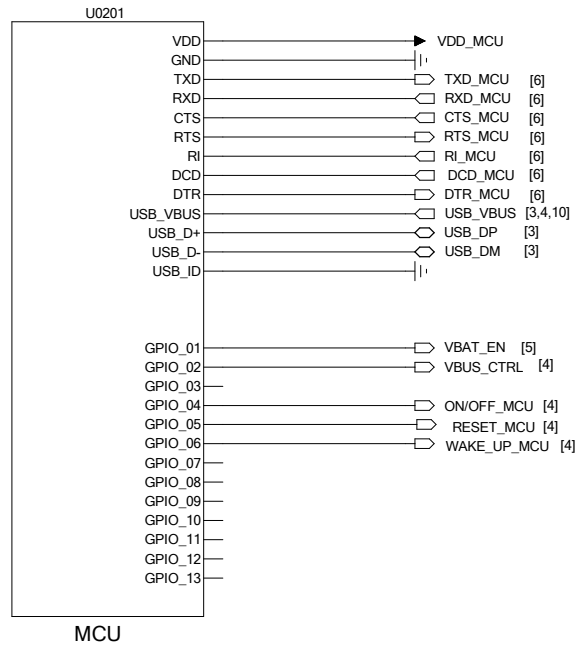| DRAWN BY Kyle CHEN/Frank WANG	PROJECT EC800G-CN	TITLE Reference Design
CHECKED BY Tiger CHENG	SIZE A2	VER 1.1
	SHEET 3 OF 10	DATE 2023/1/9

MCU Interfaces

It is used to reset the module.

RESET_N [3,10]

It is used to turn on or off the module.

PWRKEY [3,10]

[4] RESET_MCU   Q0202

U0201

VDD	VDD_MCU
GND	
TXD	TXD_MCU [6]
RXD	RXD_MCU [6]
CTS	CTS_MCU [6]
RTS	RTS_MCU [6]
RI	RI_MCU [6]
DCD	DCD_MCU [6]
DTR	DTR_MCU [6]
USB_VBUS	USB_VBUS [3,4,10]
USB_D+	USB_DP [3]
USB_D-	USB_DM [3]
USB_ID	

[4] ON/OFF_MCU   Q0201   C0201

GPIO_01   VBAT_EN [5]
GPIO_02   VBUS_CTRL [4]
GPIO_03
GPIO_04   ON/OFF_MCU [4]
GPIO_05   RESET_MCU [4]
GPIO_06   WAKE_UP_MCU [4]
GPIO_07
GPIO_08
GPIO_09
GPIO_10
GPIO_11
GPIO_12
GPIO_13

MCU

5 V power supply from motherboard.

DC_5V

USB_VBUS [3,4,10]

C0205
470nF

S   D
Q0205
G

R0204
100K

It is used to wake up the module.

MAIN_DTR [3,6]

[4] WAKE_UP_MCU   Q0203   C0202

R0203

[4] VBUS_CTRL   Q0207

NOTE:
1. U0201 represents your MCU. The power domain of GPIO interfaces of the module is 1.8 V.
   If the GPIO interfaces of U0201 share the same power domain, the related level-shifting circuit can be omitted.
2. The USB 2.0 interface of the module only serves as a slave device and supports high-speed and full-speed modes.
   To communicate with the USB interface, MCU needs to support USB host or OTG function. The USB_VBUS pin of the module
   should be powered by an external power system for USB detection, and VBUS_CTRL is used to turn on/off the USB_VBUS power supply.
3. It is recommended to select the default low-level GPIO pins of MCU as the control pins for PWRKEY and RESET_N of the module.
   Please ensure that the maximum load capacitance of pins PWRKEY and RESET_N does not exceed 10 nF.
4. When the sleep function of the module is enabled, pulling down MAIN_DTR can wake up the module from the sleep mode.You can choose either
   the open-collector control circuit or the level-shifting circuit on the "UART Design" sheet in the design.
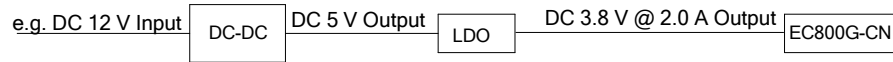   For more information, please refer to the hardware design document of the module.
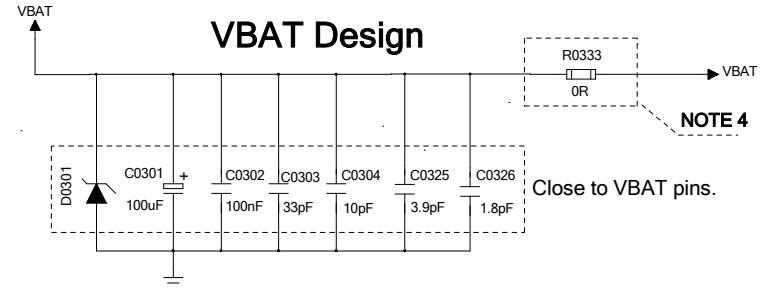
Power Supply Design

DC-DC Application

When the input voltage is above 7.0 V, use a DC-DC converter to convert the input voltage into a 5.0 V first, and then convert it to 3.8 V typical voltage with an LDO.
The rated output current of LDO must meet 2.0 A.

e.g. DC 12 V Input → DC-DC → DC 5 V Output → LDO → DC 3.8 V @ 2.0 A Output → EC800G-CN

VBAT Design

VBAT

R0333 0R → VBAT

NOTE 4

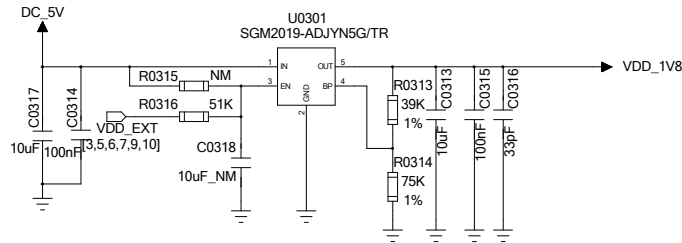D0301 | C0301 100uF | C0302 100nF | C0303 33pF | C0304 10pF | C0325 3.9pF | C0326 1.8pF | Close to VBAT pins.
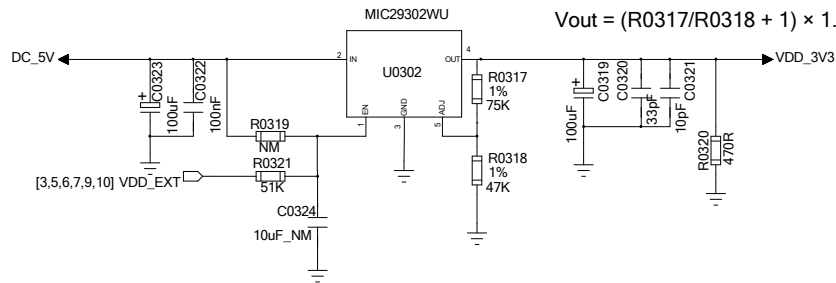
NOTE:
1. The power supply should be able to provide sufficient current up to 2.0 A for the module.
2. The width of VBAT trace should be not less than 2 mm.
3. The typical operating voltage of VBAT is 3.8 V.
4. It is recommended to reserve a 0 Ω resistor (the size should be not smaller than 0603 package) for future debugging. It needs to be placed close to VBAT pins.

Power Supply for PCM Codec

$Vout = (R0313/R0314 + 1) \times 1.207 = 1.8$ V

DC_5V

U0301 SGM2019-ADJYN5G/TR

C0317 10uF | C0314 100nF | R0315 NM | R0316 51K | VDD_EXT [3,5,6,7,9,10] | C0318 10uF_NM | R0313 39K 1% | C0313 10uF | C0315 100nF | C0316 33pF | → VDD_1V8

R0314 75K 1%

$Vout = (R0317/R0318 + 1) \times 1.24 = 3.3$ V

MIC29302WU

DC_5V | C0323 100uF | C0322 100nF | U0302 | R0319 NM | R0321 51K | R0317 1% 75K | R0318 1% 47K | C0319 100uF | C0320 33pF | C0321 10pF | R0320 470R | → VDD_3V3

[3,5,6,7,9,10] VDD_EXT | C0324 10uF_NM

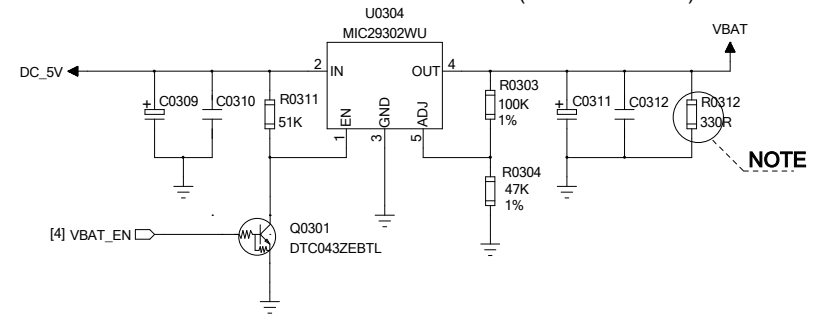**NOTE:**
VDD_EXT is used to turn on/off VDD_1V8 and VDD_3V3.

LDO Application

When the input voltage is below 7.0 V, use an LDO to convert the input voltage to 3.8 V.

$VBAT = (R0303/R0304 + 1) \times 1.24 = 3.88$ V

U0304 MIC29302WU

DC_5V | C0309 | C0310 | R0311 51K | IN | EN | GND | ADJ | OUT | R0303 100K 1% | C0311 | C0312 | R0312 330R | VBAT

NOTE

R0304 47K 1%

[4] VBAT_EN | Q0301 DTC043ZEBTL

NOTE:
The recommended load current is greater than 10 mA.

UART Design

UART Level-shifting Circuit - Transistor Solution

VDD_EXT VDD_EXT

C0401
1nF
R0401
4.7K
R0404
10K

Q0401
2SC4617TLQ

[4,6] TXD_MCU   MAIN_RXD   [3,6]

VDD_MCU   VDD_EXT

R0402
10K
R0403
4.7K
C0402
1nF

Q0402
2SC4617TLQ

[4,6] RXD_MCU   MAIN_TXD   [3,6]

UART Level-shifting Circuit - IC Solution

U0402

100nF C0404

1	A1	B1	20
2	VCCA	VCCB	19
3	A2	B2	18
4	A3	B3	17
5	A4	B4	16
6	A5	B5	15
7	A6	B6	14
8	A7	B7	13
9	A8	B8	12
10	OE	GND	11

C0405 100nF

VDD_EXT
VDD_MCU

[3]   MAIN_DCD
[3,6] MAIN_TXD
[3,6] MAIN_RXD
[3]   MAIN_RI
[3,4] MAIN_DTR
[3]   MAIN_CTS
[3]   MAIN_RTS
VDD_EXT

DCD_MCU   [4]
RXD_MCU   [4,6]
TXD_MCU   [4,6]
RI_MCU   [4]
DTR_MCU   [4]
CTS_MCU   [4]
RTS_MCU   [4]

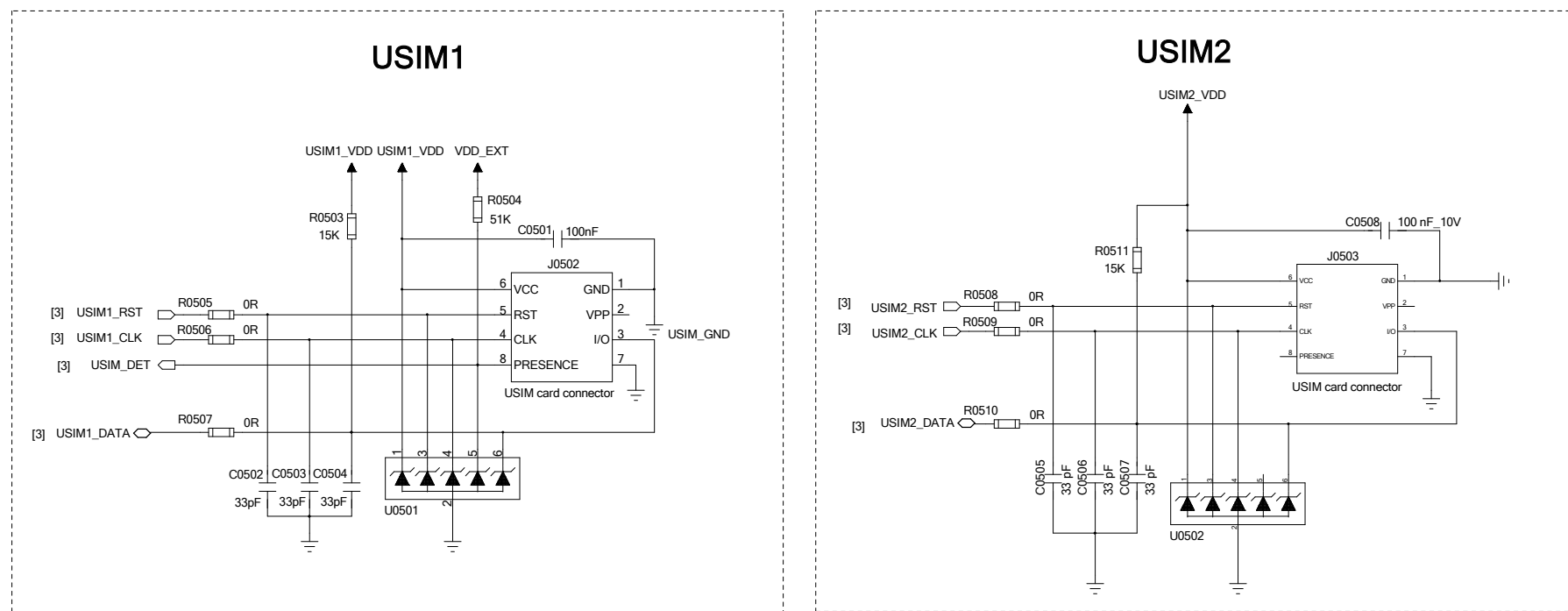10K R0410
120K R0411
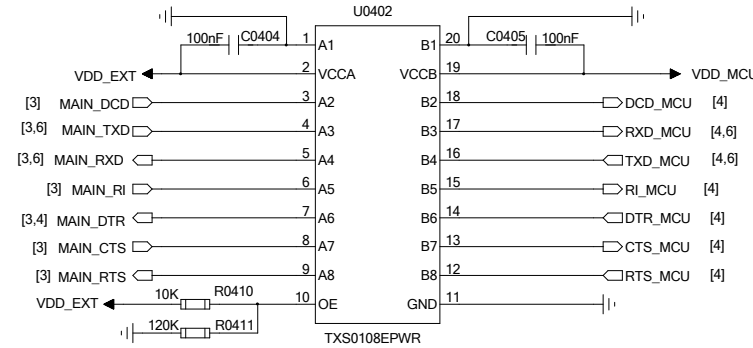
TXS0108EPWR

NOTE:
1. There are two level-shifting solutions: transistor and IC solutions, and the latter of which is recommended.
2. The power supply of TXS0108EPWR's VCCA should not exceed that of VCCB.
   For more information, please refer to the datasheet of TXS0108EPWR.
3. The transistor solution is not suitable for applications with baud rates exceeding 460 kbps.
   The 1 nF capacitors (C0401 and C0402) can improve the signal quality.
4. MAIN_RTS and MAIN_DTR level-shifting circuits are similar to that of the MAIN_RXD.
   MAIN_CTS, MAIN_RI and MAIN_DCD level-shifting circuits are similar to that of the MAIN_TXD.

USIM Interface Design

USIM1

USIM1_VDD USIM1_VDD VDD_EXT

R0503 15K
R0504 51K
C0501 100nF

J0502

6	VCC	GND	1
5	RST	VPP	2
4	CLK	I/O	3
8	PRESENCE		7

USIM card connector

[3] USIM1_RST R0505 0R
[3] USIM1_CLK R0506 0R
[3] USIM_DET
[3] USIM1_DATA R0507 0R

USIM_GND

C0502 33pF C0503 33pF C0504 33pF

U0501

USIM2

USIM2_VDD

C0508 100 nF_10V

R0511 15K

J0503

6	VCC	GND	1
5	RST	VPP	2
4	CLK	I/O	3
8	PRESENCE		7

USIM card connector

[3] USIM2_RST R0508 0R
[3] USIM2_CLK R0509 0R
[3] USIM2_DATA R0510 0R

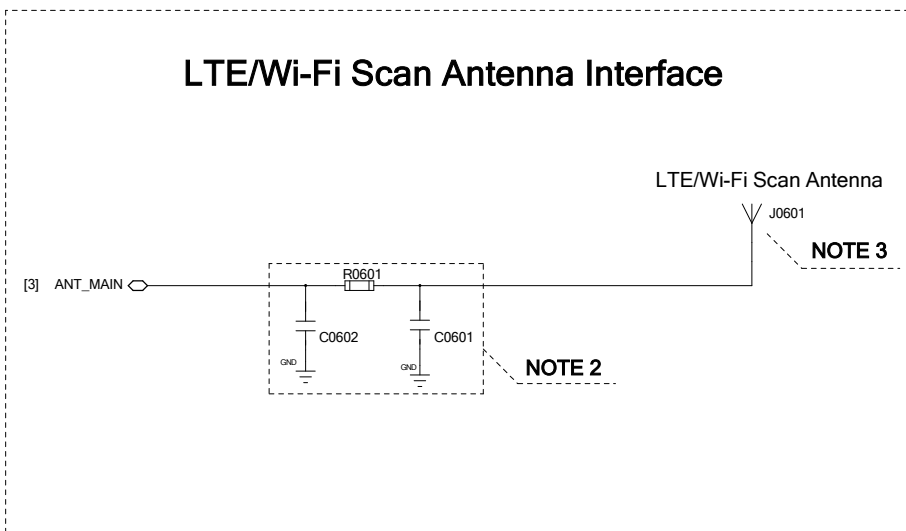C0505 33 pF C0506 33 pF C0507 33 pF

U0502

NOTE:

1. U0501 and U0502 are recommended to be used to offer good ESD protection, and the parasitic capacitance should be less than 15 pF.
2. The pull-up resistors R0503 and R0511 can improve anti-jamming capability, and should be placed close to the USIM card connector.
3. R0505-R0507 and R0508-R0510 are used for debugging, and C0502-C0504 and C0505-C0507 are used for filtering out RF interference.
4. C0501 and C0508's capacitance should be less than 1 μF and they should be placed close to the USIM card connector.
5. The GND of the USIM card connector is recommended to be connected to the GND layer directly.
6. For more information about the layout of USIM interface, please refer to the hardware design document of the module.

RF Interface Design

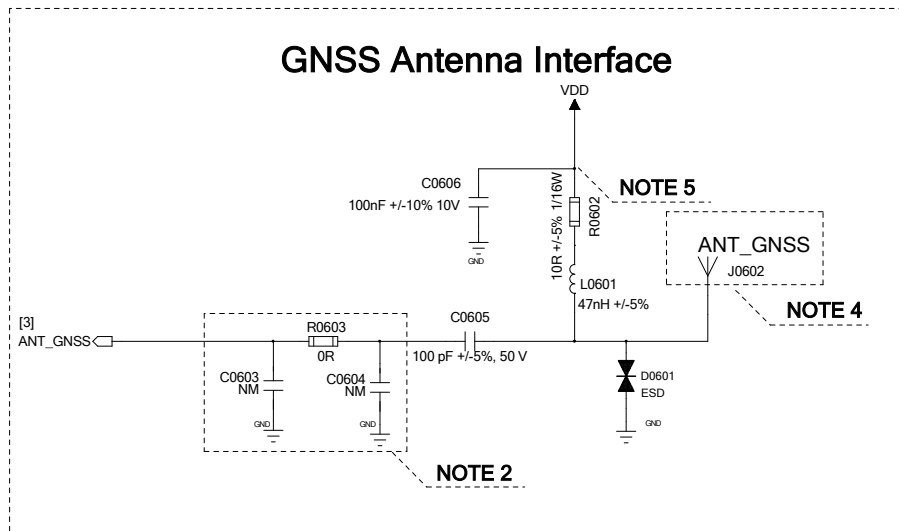## LTE/Wi-Fi Scan Antenna Interface

LTE/Wi-Fi Scan Antenna

J0601

NOTE 3

[3]   ANT_MAIN

R0601

C0602   C0601

GND   GND

NOTE 2

GNSS Antenna Interface

VDD

C0606
100nF +/-10% 10V

GND

R0602
10R +/-5% 1/16W

NOTE 5

ANT_GNSS
J0602

NOTE 4

L0601
47nH +/-5%

[3]
ANT_GNSS

R0603
0R

C0605
100 pF +/-5%, 50 V

C0603
NM

C0604
NM

D0601
ESD

GND   GND

GND

NOTE 2

NOTE:

1.The signle-ended impedance of the RF antenna is 50 Ω.

2. It is recommended to reserve a Π-type matching circuit at these antenna interfaces.

3. The Wi-Fi Scan function shares the same antenna interface with ANT_MAIN. The two functions cannot be used at the same time.

4. GNSS function is optional for the module.

5. The active antenna uses an LDO for power supply, and VDD circuit is not needed when using passive antenna.
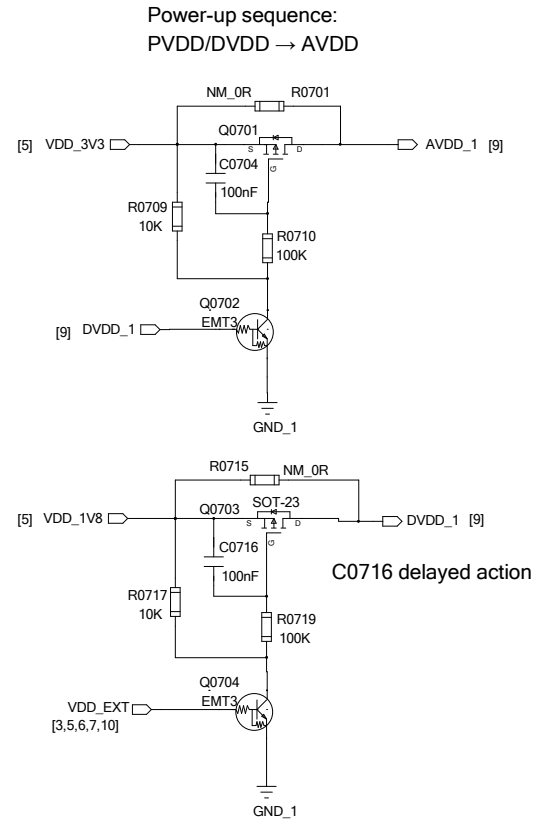
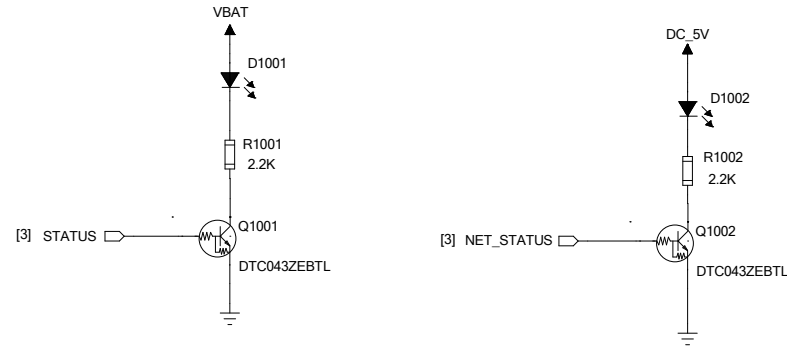# Audio Codec Design

Power-up sequence:
PVDD/DVDD → AVDD
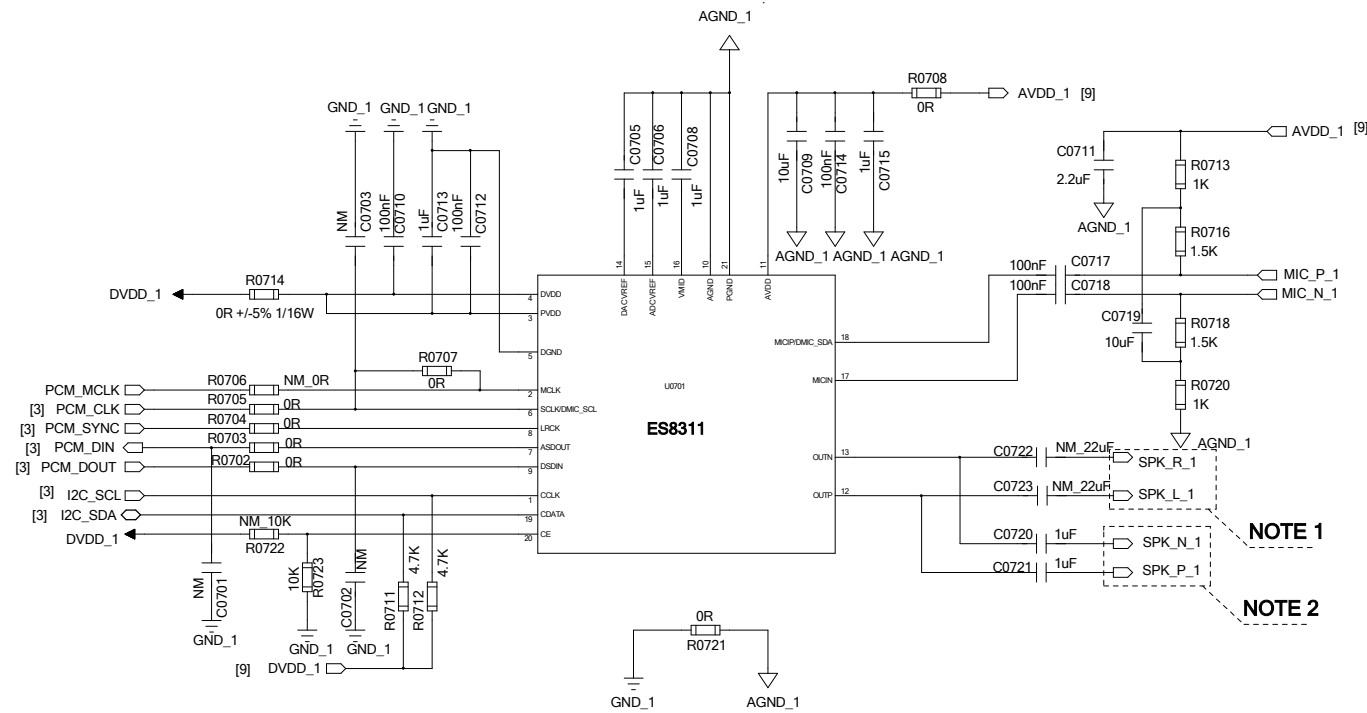
NOTE:

1. Left and right channels that can be connected to headphone.
2. Differential signal that can be connected to audio power amplifier.

NOTE 1
NOTE 2

C0716 delayed action

ES8311
U0701

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Other Design

Indicators

VBAT

D1001

R1001
2.2K

[3] STATUS   Q1001
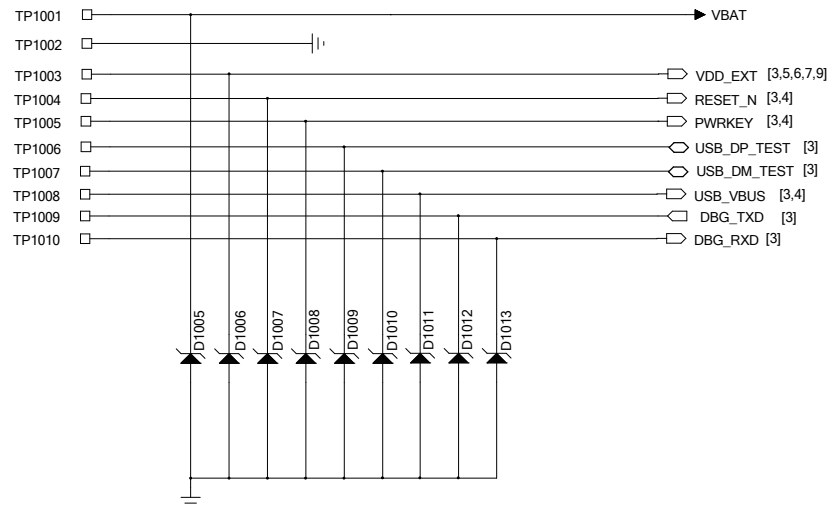DTC043ZEBTL

DC_5V

D1002

R1002
2.2K

[3] NET_STATUS   Q1002
DTC043ZEBTL

NOTE:

1. For more details about STATUS and NET_STATUS, please refer to the hardware design document of the module.

2. If low current consumption is required when your device is in sleep, replace the power supply VBAT and DC_5V of the STATUS and NET_STATUS indicators with the external controllable ones, which can be turned off when the module is in sleep mode to reduce the power consumption.
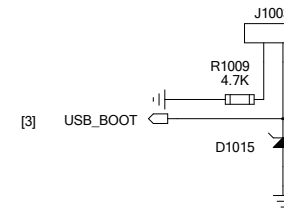
Reserved Test Points

TP1001   VBAT
TP1002
TP1003   VDD_EXT [3,5,6,7,9]
TP1004   RESET_N [3,4]
TP1005   PWRKEY [3,4]
TP1006   USB_DP_TEST [3]
TP1007   USB_DM_TEST [3]
TP1008   USB_VBUS [3,4]
TP1009   DBG_TXD [3]
TP1010   DBG_RXD [3]

D1005 D1006 D1007 D1008 D1009 D1010 D1011 D1012 D1013

NOTE:

1. Test points for both USB and debug UART interfaces must be reserved for catching logs.

2. Test points for USB interface can also be reserved for firmware upgrade.

3. The parasitic capacitance of the ESD protection components on USB data traces should be less than 2 pF.

4. The debug UART interface supports 1.8 V power domain, and a voltage-level translator should be used if the power domain of your application is 3.3 V.

5. Test points are recommended to be reserved for RESET_N and VDD_EXT.

Emergency Download

J1003

R1009
4.7K

[3] USB_BOOT

D1015

NOTE:

1. Ensure to reserve the USB_BOOT interface design and a test point is recommended to be reserved.

2. You can pull down USB_BOOT to GND before the module is turned on, and the module will enter emergency download mode when it is turned on. In this mode, the module supports firmware upgrade over USB interface.

Quectel Wireless Solutions		
DRAWN BY Kyle CHEN/Frank WANG	PROJECT EC800G-CN	TITLE Reference Design
CHECKED BY Tiger CHENG	SIZE A2	VER 1.1
	SHEET 10 OF 10	DATE 2023/1/9