EG915N Series

Hardware Design

LTE Standard Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2021-11-19	Shihao HUANG/ Jeff SHEN	Creation of the document
1.0	2022-02-25	Shihao HUANG/ Jeff SHEN	First official release
1.1	2022-10-14	Shihao HUANG/ Evan ZOU/ Yule Deng	1. Added a new variant EG915N-LA and related information. 2. Updated the weight of the module. (Table 2) 3. Added dual SIM single Standby function. (Table 3 and Chapter 3.9) 4. Updated the USB serial drivers. (Table 3) 5. Added the emergency call function. (Table 3) 6. Added the normal voltage in DC characteristics of PWRKEY and RESET_N. (Table 7) 7. Updated the reference design of power supply. (Figure 8) 8. Updated the power-down timing. (Figure 13) 9. Updated the reference design of microphone interface. (Figure 22) 10. Deleted the information on long frame mode and the PCM interface used as slave device in short frame mode. (Chapter 3.13) 11. Updated reference design of PCM and I2C applications. (Figure 26) 12. Updated GNSS frequency range. (Table 32) 13. Updated the digital I/O characteristics. (Chapter 6.3) 14. Updated the power consumption of the module. (Table 39)

	15. Updated the ramp-up slope, cool-down slope and the note. (Chapter 8.2)

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1 Introduction

This document defines the EG915N series module and describes its air interface and hardware interfaces which are connected with your applications.

This document can help you quickly understand module interface specifications, electrical and mechanical details, as well as other related information of the module. Associated with application notes and user guides, you can use the module to design and set up wireless applications easily.

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, an asterisk (*) after a function, feature, interface, pin name, AT command, or argument indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of the model is currently unavailable.

2 Product Overview

The module is an SMD type module which is engineered to meet most of the requirements for M2M applications such as automation, metering, tracking system, security, router, wireless POS, mobile computing device, PDA phone, tablet PC, etc.

Table 2: Brief Introduction of the Module

Categories	
Packaging and pins number	126 LGA Pins
Dimensions	(23.6 ±0.2) mm × (19.9 ±0.2) mm × (2.4 ±0.2) mm
Weight	Approx. 2.46 g

2.1. Frequency Bands and Functions

Table 3: Frequency Bands of EG915N-EU

Mode	Frequency Bands
LTE-FDD	B1/B3/B7/B8/B20
GSM	EGSM900/DCS1800
GNSS (Optional)	GPS/GLONASS/Galileo/BDS/QZSS/SBAS

Table 4: Frequency Bands of EG915N-LA

Mode	Frequency Bands
LTE-FDD	B2/B3/B4/B5/B7/B8/B28/B66
GSM	GSM850/EGSM900/DCS1800/PCS1900
GNSS (Optional)	GPS/GLONASS/Galileo/BDS/QZSS/SBAS

2.2. Key Features

The following table describes the detailed features of the module.

Table 5: Key Features

Features	Details
Power Supply	● Supply voltage: 3.4–4.5 V ● Typical supply voltage: 3.8 V
Transmitting Power	● Class 4 (33 dBm ±2 dB) for GSM850 ● Class 4 (33 dBm ±2 dB) for EGSM900 ● Class 1 (30 dBm ±2 dB) for DCS1800 ● Class 1 (30 dBm ±2 dB) for PCS1900 ● Class E2 (27 dBm ±3 dB) for GSM850 8-PSK ● Class E2 (27 dBm ±3 dB) for EGSM900 8-PSK ● Class E2 (26 dBm ±3 dB) for DCS1800 8-PSK ● Class E2 (26 dBm ±3 dB) for PCS1900 8-PSK ● Class 3 (23 dBm ±2 dB) for LTE-FDD bands
LTE Features	● Supports up to Cat 1 FDD ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth ● LTE-FDD: Max. 10 Mbps (DL), Max. 5 Mbps (UL)
GSM Features	**GPRS:** ● Supports GPRS multi-slot class 12 ● Coding scheme: CS 1–4 ● Max. 85.6 kbps (DL), Max. 85.6 kbps (UL) **EDGE:** ● Supports EDGE multi-slot class 12 ● Supports GMSK and 8-PSK for different MCS ● Downlink coding schemes: MCS 1–9 ● Uplink coding schemes: MCS 1–9 ● Max. 236.8 kbps (DL), Max. 236.8 kbps (UL)

Internet Protocol Features	● Supports TCP/UDP/PPP/FTP/HTTP/NTP/PING/NITZ/CMUX/HTTPS/ SMTP/MMS/FTPS/SMTPS/SSL/FILE/MQTT protocols ● Supports PAP and CHAP for PPP connections
SMS	● Text and PDU modes ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: (U)SIM card and ME, ME by default
(U)SIM Interfaces	● Supports (U)SIM card: 1.8/3.0 V ● Supports Dual SIM Single Standby
Audio Features	● Supports one digital audio interface: PCM interface ● Supports one analog audio input and one analog audio output ● GSM: HR/FR/EFR/AMR/AMR-WB ● Supports echo cancellation and noise suppression
PCM Interface	● Used for audio function with an external codec ● Short frame mode: module can only be used as master device
USB Interface	● Compliant with USB 2.0 specification (slave only), with data transmission rate up to 480 Mbps ● Used for AT command communication, data transmission, software debugging and firmware upgrade ● Supports USB serial drivers for: Windows 7/8/8.1/10/11, Linux 2.6–5.18, Android 4.x–12.x, etc.
UART Interfaces	**Main UART:** ● Used for AT command communication and data transmission ● Baud rate: 115200 bps by default ● Supports RTS and CTS hardware flow control **Auxiliary UART*:** ● Supports RTS and CTS hardware flow control **Debug UART:** ● Used for the output of partial logs ● Baud rate:115200 bps
AT Commands	Compliant with *3GPP TS 27.007, 3GPP TS 27.005* and Quectel enhanced AT commands
Network Indication	NET_STATUS to indicate the network connectivity status
Antenna Interfaces	● Main antenna interface (ANT_MAIN) ● GNSS antenna interface (ANT_GNSS) [1] ● 50 Ω impedance
Position Fixing	● Supports Wi-Fi scan and shares the main antenna

[1] GNSS function is optional for the module. Only the module with built-in GNSS function can support GNSS positioning function.

	• Supports GNSS positioning [1]
Operating Temperature	• Operating temperature range: -35 °C to +75 °C [2] • Extended temperature range: -40 °C to +85 °C [3] • Storage temperature range: -40 °C to +90 °C
Firmware Upgrade	Via USB interface or DFOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

2.3. Functional Diagram

The following figure shows a block diagram of the module and illustrates the major functional parts.

- Power management
- Baseband
- Memory
- Radio frequency
- Peripheral interfaces

[2] Within operating temperature range, the module is 3GPP compliant.
[3] Within extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission, emergency call, etc, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

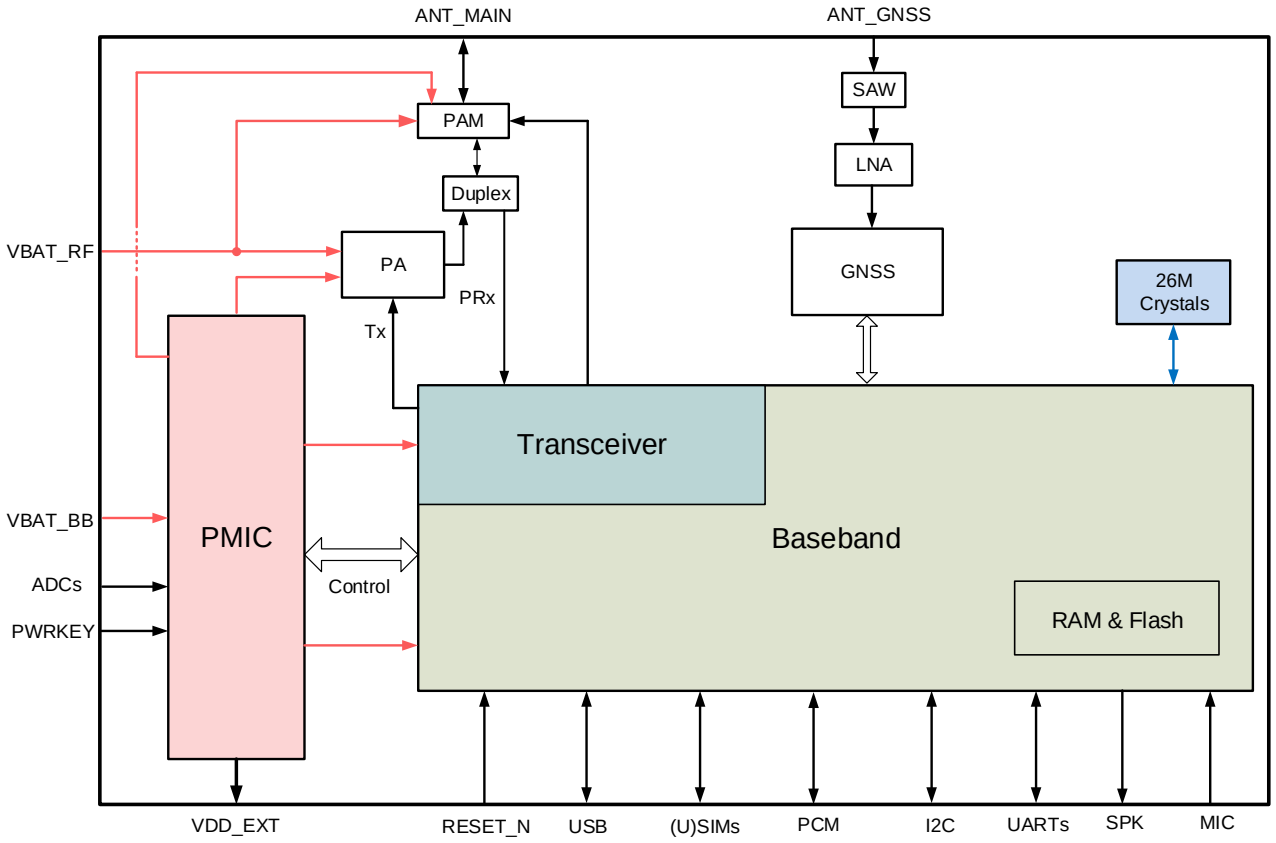


Figure 1: Functional Diagram of EG915N Series

2.4. EVB Kit

To help you develop applications with the module, Quectel supplies an evaluation board (UMTS & LTE EVB) with accessories to control or test the module. For more details, see ***document [1]***.

3 Application Interfaces

3.1. General Description

The module is equipped with 126 LGA pins that can be connected to cellular application platform. The subsequent chapters will provide detailed descriptions of the following interfaces.

- Power supply
- (U)SIM interfaces
- USB interface
- UART interfaces
- Analog audio interfaces
- PCM and I2C interfaces
- Network status indication
- USB_BOOT interface
- STATUS
- ADC interfaces

3.2. Pin Assignment

The following figure shows the pin assignment of the module.

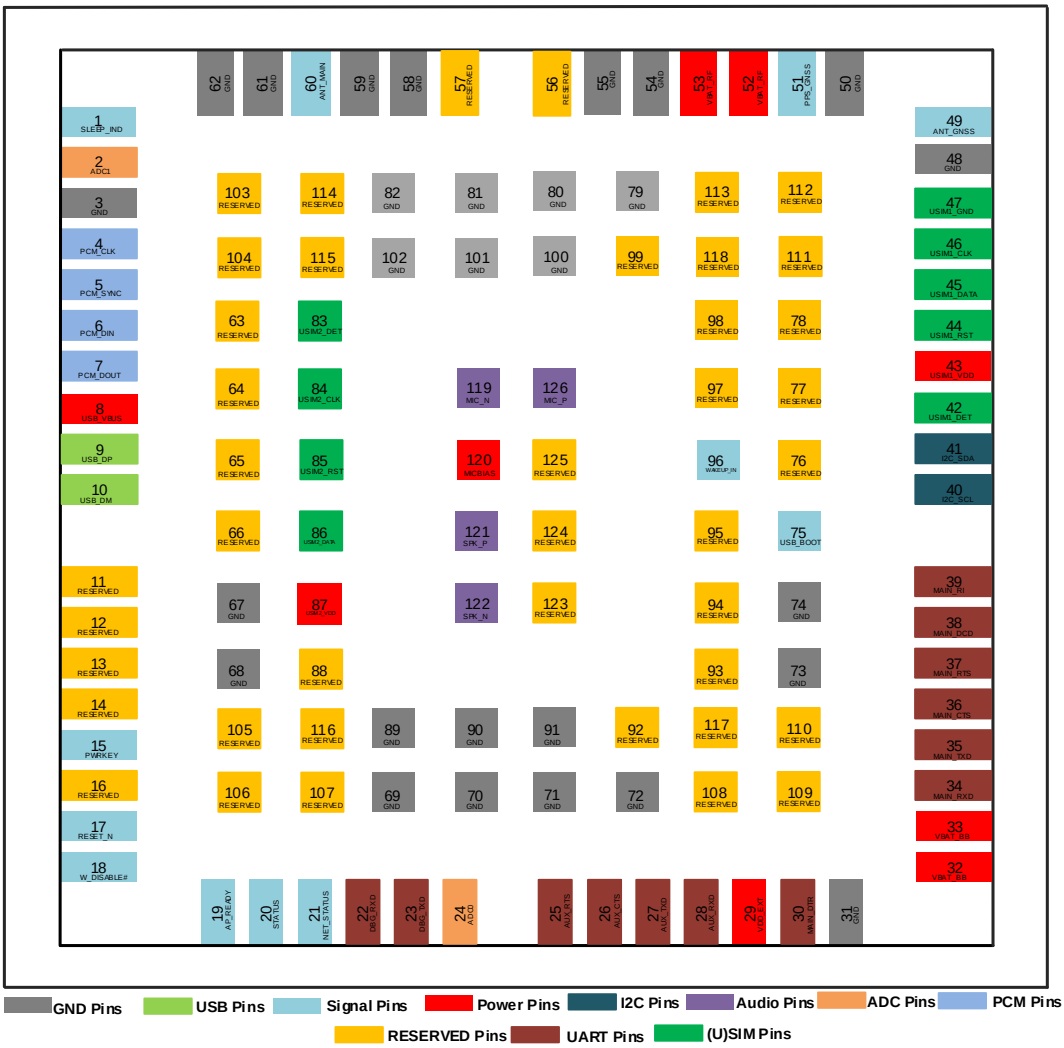


Figure 2: Pin Assignment (Top View)

NOTE

1. For EG915N-EU, pin 2 and pin 24 are ADC pins; for EG915N-LA, pin 2 and pin 24 are RESERVED pins.
2. All GND pins should be connected to ground, and keep unused and RESERVED pins unconnected.
3. USB_BOOT cannot be pulled up to high level before the module is successfully startup.
4. ANT_GNSS and PPS_GNSS are the GNSS pins for the module with built-in GNSS function.
5. Ensure that there is a complete reference ground plane below the module, and the ground plane is as close to the module layer as possible. At least a 4-layer board design is recommended.

3.3. Pin Description

The following tables show the pin definition and description of the module.

Table 6: I/O Parameters Definition

Type	Description
AI	Analog Input
AIO	Analog Input/Output
AO	Analog Output
DI	Digital Input
DO	Digital Input/Output
DIO	Digital Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics include power domain and rate current, etc.

Table 7: Pin Description

Power Supply Input					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	32, 33	PI	Power supply for the module's baseband part	Vmax = 4.5 V Vmin = 3.4 V Vnom = 3.8 V	It must be provided with sufficient current up to 0.8 A.
VBAT_RF	52, 53	PI	Power supply for the module's RF part		It must be provided with sufficient current up to 2.2 A.
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–102				
Power Supply Output					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
VDD_EXT	29	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull-up circuits. If unused, keep it open.
Turn On/Off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	15	DI	Turn on/off the module	V_{IL}max = 0.5 V Vnom = VBAT	VBAT power domain.
RESET_N	17	DI	Reset the module	V_{IL}max = 0.5 V Vnom = 1.8 V	Active low. 1.8 V power domain. If unused, keep it open.
Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SLEEP_IND	1	DO	Indicate the module's sleep mode	1.8 V	If unused, keep them open.
STATUS	20	DO	Indicate the module's operation status		
NET_STATUS	21	DO	Indicate the module's network activity status		
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	8	AI	USB connection detect	Vmax = 5.25 V Vmin = 3.0 V Vnom = 5.0 V	If unused, keep it open.
USB_DP	9	AIO	USB differential data (+)		Requires differential impedance of 90 Ω. USB 2.0 compliant. If unused, keep them open.
USB_DM	10	AIO	USB differential data (-)		
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

USIM1_DET	42	DI	(U)SIM1 card hot-swap detect	1.8 V	If unused, keep it open.
USIM1_VDD	43	PO	(U)SIM1 card power supply	$I_O$max = 50 mA 1.8/3.0 V	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM1_RST	44	DO	(U)SIM1 card reset	USIM1_VDD 1.8/3.0 V	
USIM1_DATA	45	DIO	(U)SIM1 card data		
USIM1_CLK	46	DO	(U)SIM1 card clock		
USIM1_GND	47		Specified ground for (U)SIM1		Connect to main GND of PCB.
USIM2_DET	83	DI	(U)SIM2 card hot-swap detect	1.8 V	If unused, keep it open.
USIM2_CLK	84	DO	(U)SIM2 card clock	USIM2_VDD 1.8/3.0 V	
USIM2_RST	85	DO	(U)SIM2 card reset		
USIM2_DATA	86	DIO	(U)SIM2 card data		
USIM2_VDD	87	PO	(U)SIM2 card power supply	$I_O$max = 50 mA 1.8/3.0 V	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.

Main UART Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
MAIN_DTR	30	DI	Main UART data terminal ready	1.8 V	If unused, keep them open.
MAIN_RXD	34	DI	Main UART receive		
MAIN_TXD	35	DO	Main UART transmit		
MAIN_CTS	36	DO	DTE clear to send signal from DCE		Connect to DTE's CTS. If unused, keep it open.
MAIN_RTS	37	DI	DTE request to send signal to DCE		Connect to DTE's RTS.

					If unused, keep it open.
MAIN_DCD	38	DO	Main UART data carrier detect		If unused, keep them open.
MAIN_RI	39	DO	Main UART ring indication		
Auxiliary UART Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
AUX_RTS	25	DI	DTE request to send signal to DCE	1.8 V	Connect to DTE's RTS. If unused, keep it open.
AUX_CTS	26	DO	DTE clear to send signal from DCE		Connect to DTE's CTS. If unused, keep it open.
AUX_TXD	27	DO	Auxiliary UART transmit		If unused, keep them open.
AUX_RXD	28	DI	Auxiliary UART receive		
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	22	DI	Debug UART receive	1.8 V	If unused, keep them open.
DBG_TXD	23	DO	Debug UART transmit		
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	24	AI	General-purpose ADC interface	Voltage range: 0 V to VBAT_BB	If unused, keep them open. EG915N-LA does not support ADC function.
ADC1	2	AI	General-purpose ADC interface		
PCM & I2C Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_CLK	4	DO	PCM clock	1.8 V	If unused, keep them

PCM_SYNC	5	DO	PCM data frame sync		open.
PCM_DIN	6	DI	PCM data input		
PCM_DOUT	7	DO	PCM data output		
I2C_SCL	40	OD	I2C serial clock		An external 1.8 V pull-up resistor is required. If unused, keep them open.
I2C_SDA	41	OD	I2C serial data		
Analog Audio Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MICBIAS	120	PO	Bias voltage output for microphone		If unused, keep them open.
MIC_N	119	AI	Microphone analog input (-)		
MIC_P	126	AI	Microphone analog input (+)		
SPK_P	121	AO	Analog audio differential output (+)		The interface can drive 32 Ω earpiece with power rate at 37 mW. It can also be used to drive external power amplifier devices if the output power rate cannot meet the demand. If unused, keep them open.
SPK_N	122	AO	Analog audio differential output (-)		
RF Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	60	AIO	Main antenna interface		50 Ω impedance.
ANT_GNSS	49	AI	GNSS antenna interface		50 Ω impedance. If unused, keep it open.
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

WAKEUP_IN*	96	DI	Wake up the module	1.8 V	If unused, keep them open.
AP_READY	19	DI	Application processor ready		
W_DISABLE#	18	DI	Airplane mode control		Pull-up by default. In low voltage level, module can enter airplane mode. If unused, keep it open.
USB_BOOT	75	DI	Force the module into emergency download mode		Active high. It is recommended to reserve test points.
PPS_GNSS	51	DO	PPS output		Cannot pull it down when GNSS function is active.

Reserved Pins		
Pin Name	**Pin No.**	**Comment**
RESERVED	11–14, 16, 56, 57, 63–66, 76–78, 88, 92–95, 97–99, 103–118, 123–125	Keep them open.

NOTE

1. ANT_GNSS and PPS_GNSS are the GNSS pins for the module with built-in GNSS function. See ***Chapter 5.2*** for details about GNSS antenna interfaces.
2. For EG915N-LA, pin 2 and pin 24 are RESERVED pins.

3.4. Operating Modes

Table 8: Overview of Operating Modes

Modes	Details	
Full Functionality Operation	Idle	Software is active. The module remains registered on the network, and it is ready to send and receive data.
	Voice/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transmission rate.
Minimum Functionality	**AT+CFUN=0** can set the module into a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card will be	

Mode	invalid.
Airplane Mode	**AT+CFUN=4** or W_DISABLE# pin can set the module to airplane mode. In this case, RF function will be invalid.
Sleep Mode	In this mode, the power consumption of the module is reduced to the minimal level. During this mode, the module can still receive paging message, SMS, voice call and TCP/UDP data from the network normally.
Power Down Mode	In this mode, the module's power supply is cut off by its power management IC. The software is inactive and the UART interfaces are not accessible, while the VBAT_RF and VBAT_BB pins are still powered.

For more information about the AT command, see ***document [2]*** for details.

3.5. Power Saving

3.5.1. Sleep Mode

The module is able to reduce its power consumption to a minimal level during sleep mode. The following section describes ways to let the module enter sleep mode.

3.5.1.1. UART Application Scenario

If the host communicates with module via UART interfaces, the following preconditions should be met at the same time to let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Drive MAIN_DTR high or keep it open.

The following figure shows the connection between the module and the host.

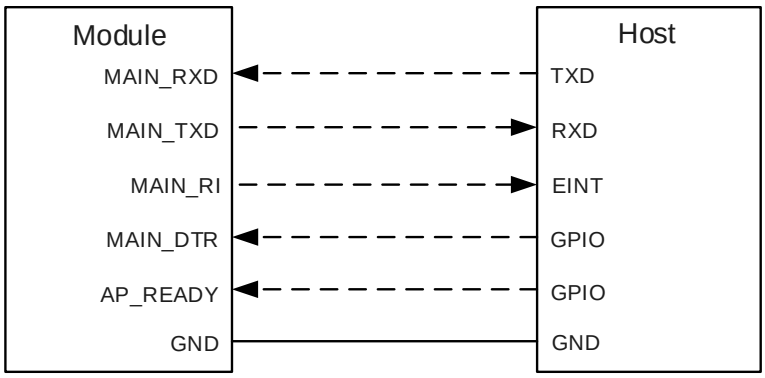


Figure 3: Sleep Mode Application via UART

- Drive MAIN_DTR low by host will wake up the module.
- When the module has a URC to report, the URC will trigger the behavior of MAIN_RI pin. See ***Chapter 3.18*** for details about MAIN_RI behaviors.

3.5.1.2. USB Application with USB Remote Wakeup Function

If the host supports USB suspend/resume and remote wakeup functions, the following three preconditions must be met at the same time to let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable the sleep mode.
- Ensure the MAIN_DTR is held at high level or keep it open.
- The host's USB bus, which is connected with the module's USB interface, enters suspend state.

The following figure shows the connection between the module and the host.

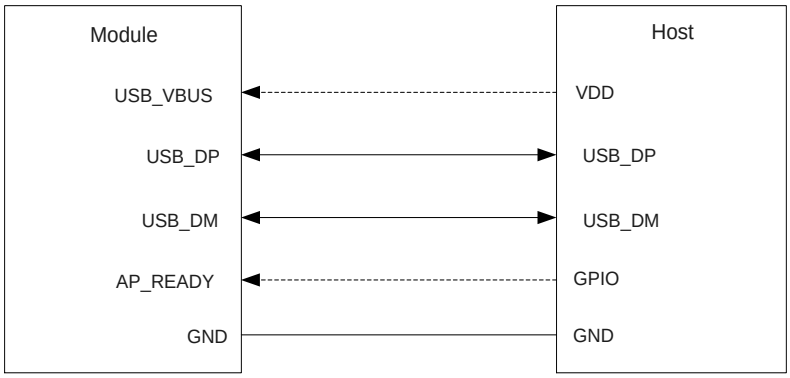


Figure 4: Sleep Mode Application with USB Remote Wakeup Function

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, the module sends remote wake-up signals to wake up the host via USB bus.

3.5.1.3. USB Application with USB Suspend/Resume and RI Function

If the host supports USB suspend/resume, but does not support remote wakeup function, the MAIN_RI signal is needed to wake up the host. The following three preconditions must be met at the same time to let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable the sleep mode.
- Ensure the MAIN_DTR is held at high level or keep it open.
- The host's USB bus, which is connected with the module's USB interface, enters suspend state.

The following figure shows the connection between the module and the host.

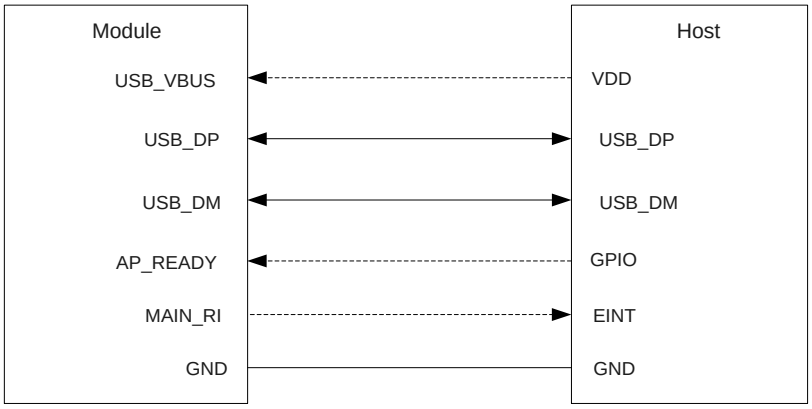


Figure 5: Sleep Mode Application with MAIN_RI

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, the URC will trigger the behavior of MAIN_RI pin. See ***Chapter 3.18*** for details about MAIN_RI behavior.

3.5.1.4. USB Application without USB Suspend Function

If the host does not support USB suspend function, disconnect USB_VBUS with an external control circuit to let the module enter sleep mode. The following three preconditions must be met at the same time to let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable the sleep mode.
- Ensure the MAIN_DTR is held at high level or keep it open.
- Disconnect the USB_VBUS power supply.

The following figure shows the connection between the module and the host.

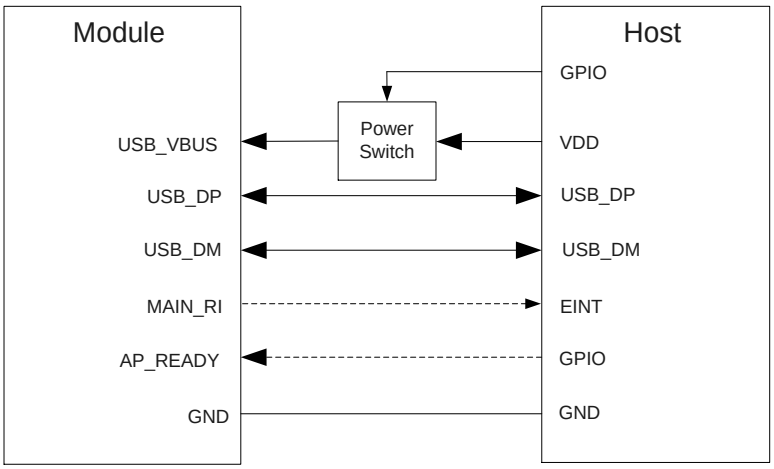


Figure 6: Sleep Mode Application without USB Suspend Function

You can wake up the module by turning on the power switch to supply power to USB_VBUS.

NOTE

1. Pay attention to the level match shown in dotted line between the module and the host in the circuit diagrams of ***Chapter 3.5.1***.
2. For more information about the AT command, see ***document [2]*** for details.

3.5.2. Airplane Mode

When the module enters airplane mode, the RF function does not work and all AT commands related to the RF function are inaccessible. The following ways can be used to let the module enter airplane mode.

Hardware:

The W_DISABLE# pin is pulled up by default. Its control function for airplane mode is disabled by default, and **AT+QCFG="airplanecontrol",1** can be used to enable the function. Driving the pin low after its control function for airplane mode is enabled by AT command, which can make the module enter the airplane mode.

Software:

AT+CFUN=<fun> provides the choice of the functionality level through setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0:** Minimum functionality mode (disable (U)SIM and RF functions).
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** Airplane mode (disable RF function).

3.6. Power Supply

3.6.1. Power Supply Pins

The module provides four VBAT pins dedicated to connecting with the external power supply. There are two separate voltage domains for VBAT.

- Two VBAT_RF pins for module's RF part
- Two VBAT_BB pins for module's baseband part

Table 9: Power Supply and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	52, 53	Power supply for the module's RF part	3.4	3.8	4.5	V
VBAT_BB	32, 33	Power supply for the module's baseband part	3.4	3.8	4.5	V
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–102					

3.6.2. Voltage Stability Requirements

The power supply range of the module is from 3.4 V to 4.5 V. Please make sure that the input voltage never drops below 3.4 V. The following figure shows the voltage drop during burst transmission in 2G network. The voltage drop will be less in 4G networks.

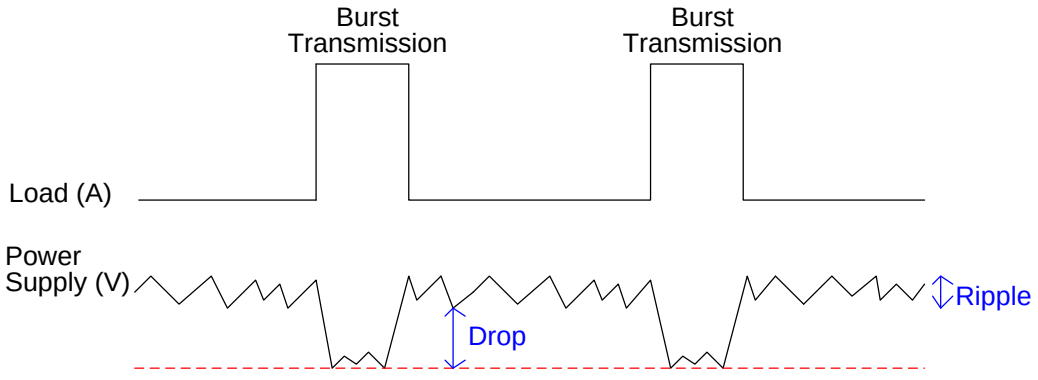


Figure 7: Power Supply Limits during Burst Transmission

To decrease voltage drop, a bypass capacitor of about 100 μF with low ESR (ESR ≤ 0.7 Ω) should be used. It is recommended to reserve three multi-layer ceramic chip (MLCC) capacitors (100 nF, 33 pF and 10 pF) with the best ESD performance, and place these capacitors close to the VBAT_BB and VBAT_RF pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star configuration. The width of VBAT_BB trace should be not less than 1 mm; and the width of VBAT_RF trace should be not less than 2 mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, in order to ensure the stability of power source, it is suggested that a WS4.5D3HV TVS diode of which reverse stand-off voltage is 4.7 V and peak pulse power is up to 2550 W should be used. The following figure shows the star configuration of the power supply.

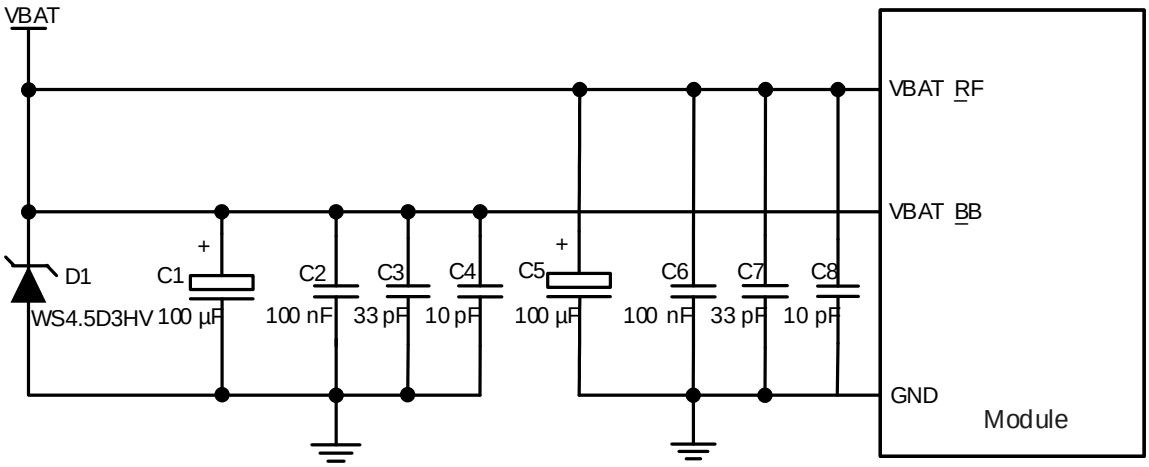


Figure 8: Reference Design of Power Supply

3.6.3. Reference Design for Power Supply

Power design for the module is very important, as the performance of the module largely depends on the power source. The power supply should be able to provide sufficient current up to 3.0 A to the module. If the voltage drop between the input and output is not too high, it is suggested that an LDO should be used. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used.

The following figure shows a reference design for +5 V input power source. The circuit is designed using the LDO of Micrel's MIC29302WU. The typical output of the power supply is about 3.8 V and the maximum load current is 3.0 A.

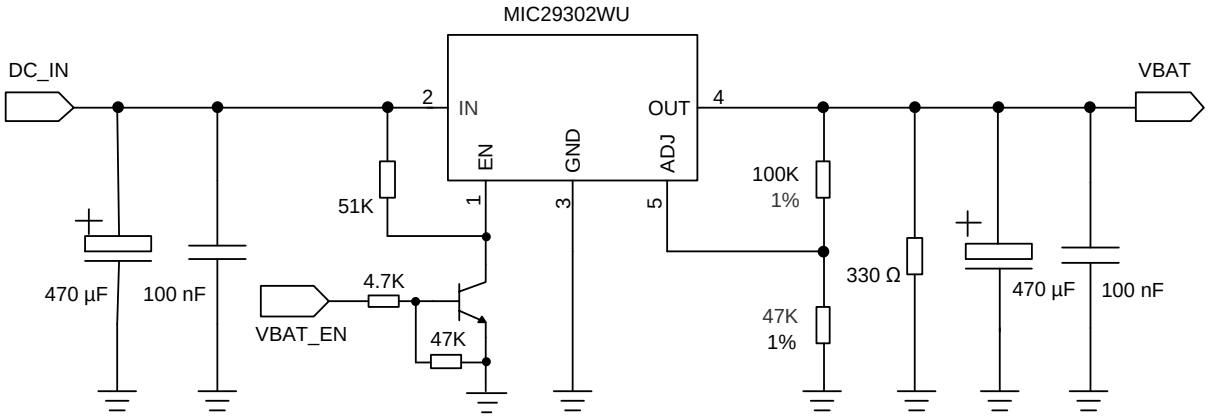


Figure 9: Reference Design of Power Supply

3.7. Turn On and Turn Off

3.7.1. Turn On with PWRKEY

Table 10: Pin Description of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	15	DI	Turn on/off the module	VBAT power domain.

When the module is in power down mode, you can turn it on to normal mode by driving the PWRKEY pin low for at least 500 ms. It is recommended to use an open drain/collector driver to control the PWRKEY.

A simple reference design is illustrated in the following figure.

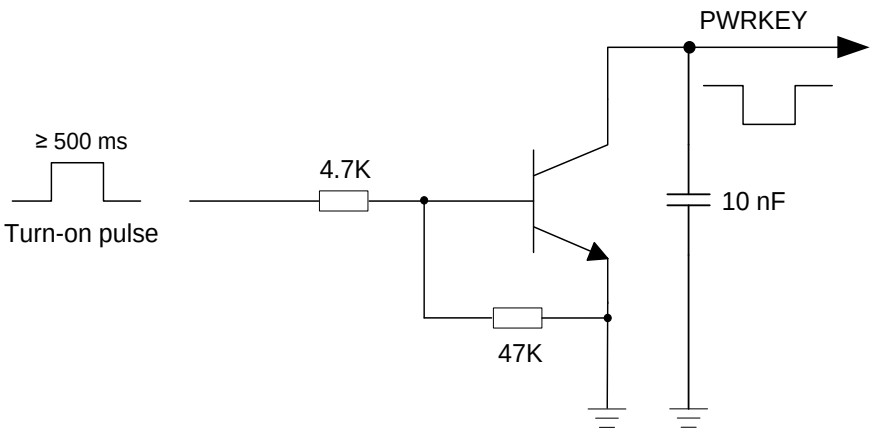


Figure 10: Reference Design of Turning on the Module with Driving Circuit

Another way to control the PWRKEY is using a button directly. a TVS diode is indispensable to be placed nearby the button for ESD protection. A reference design is shown in the following figure.

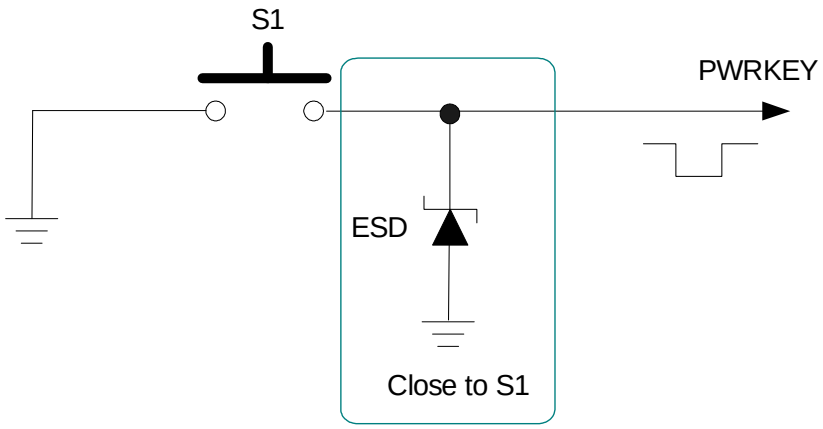


Figure 11: Reference Design of Turning on the Module with a Button

The timing of turning on the module is illustrated in the following figure.

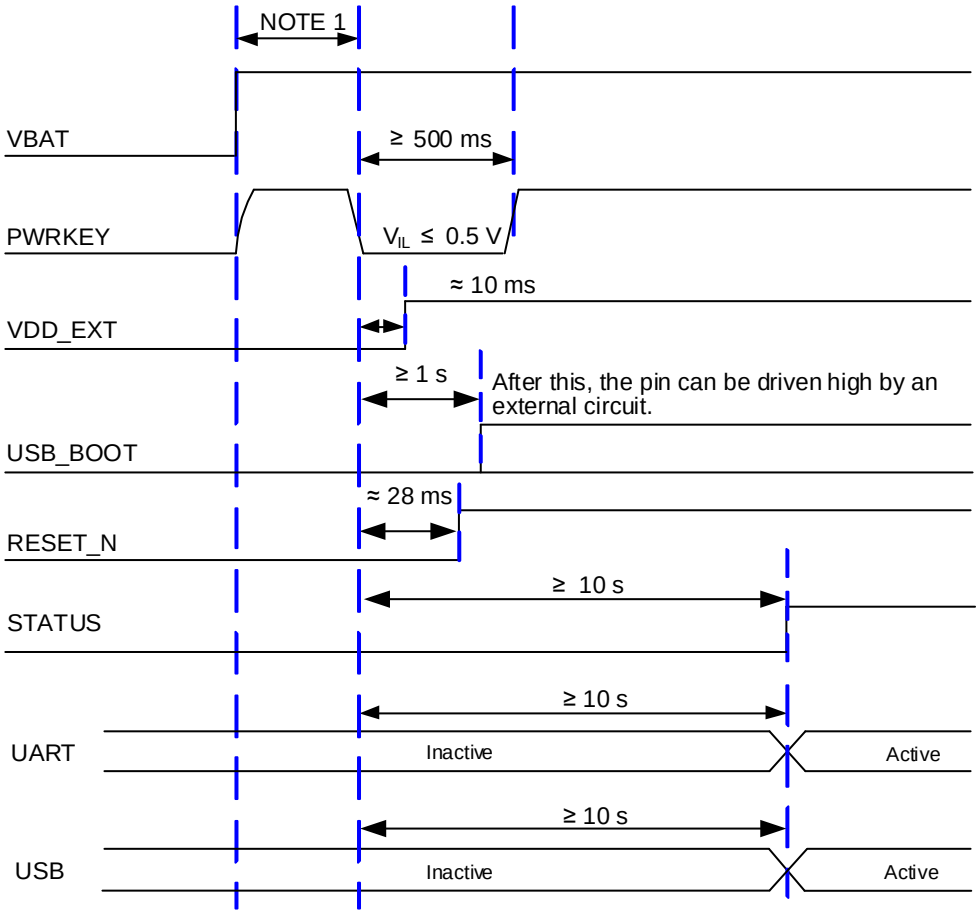


Figure 12: Power Up Timing

NOTE

1. Ensure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time difference between powering up VBAT and pulling down PWRKEY pin is not less than 30 ms.
2. PWRKEY can be pulled down directly to GND with a recommended 4.7 kΩ resistor if the module needs to be turned on automatically and shutdown is not needed.

3.7.2. Turn Off

The following procedures can be used to turn off the module normally:

- Use the PWRKEY pin.
- Execute **AT+QPOWD**.

3.7.2.1. Turn off with PWRKEY

Drive the PWRKEY pin low for at least 650 ms and then release it. After this, the module executes power-down procedure. The timing of turning off the module is illustrated in the following figure.

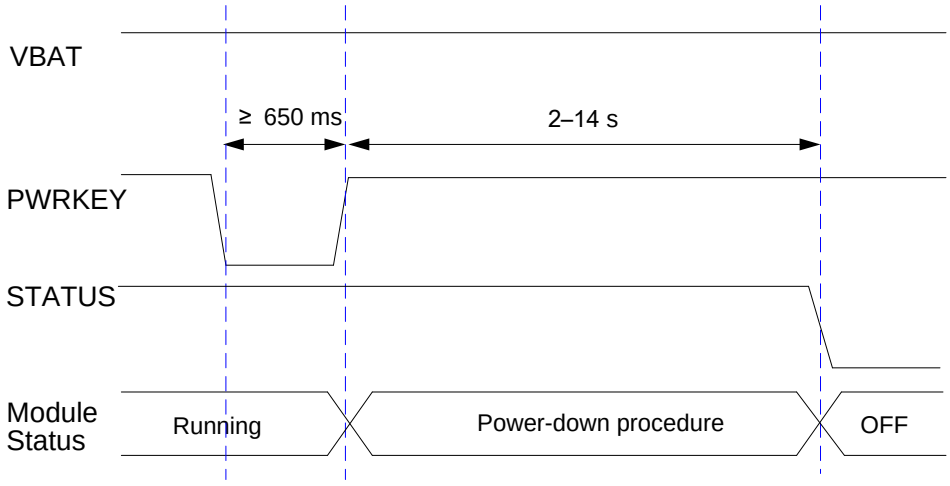


Figure 13: Power Down Timing

3.7.2.2. Turn off with AT Command

It is also a safe way to use **AT+QPOWD** to turn off the module, which is similar to the procedure of turning off the module via PWRKEY pin. See ***document [2]*** for details about **AT+QPOWD**.

NOTE

1. To avoid corrupting the data in the internal flash, do not switch off the power supply when the module works normally. Only after the module is shut down with PWRKEY or AT command, can the power supply be cut off.
2. When turning off module with the AT command, keep PWRKEY at high level after the execution of the command. Otherwise, the module will turn on again after successful turn-off.

3.8. Reset

The RESET_N pin can be used to reset the module. You can reset the module by driving RESET_N low for at least 300 ms and then releasing it. The RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 11: Pin Description of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	17	DI	Reset the module	Active low. 1.8 V power domain. If unused, keep it open.

The recommended design is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control RESET_N.

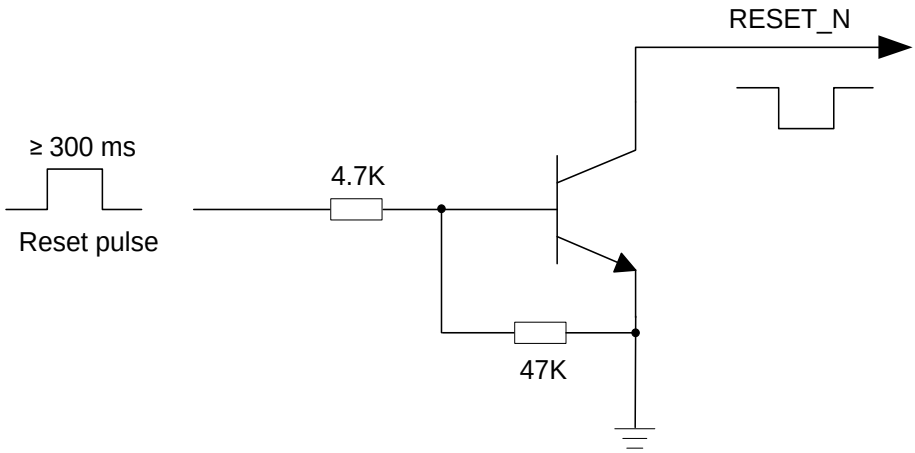


Figure 14: Reference Design of RESET_N with Driving Circuit

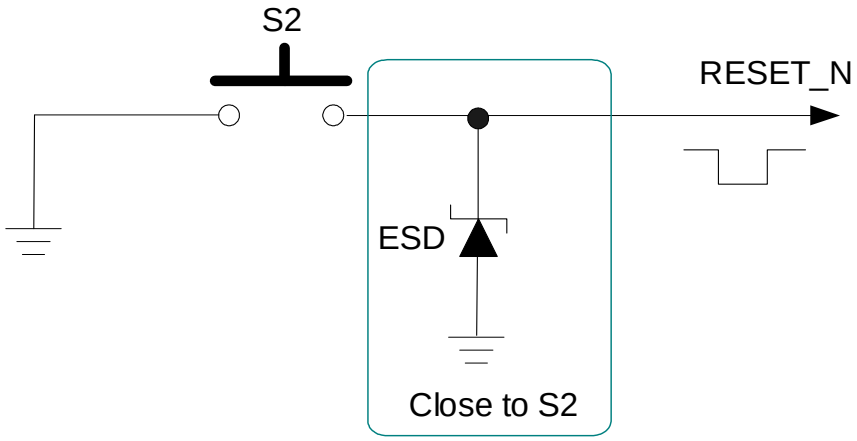


Figure 15: Reference Design of RESET_N with a Button

The reset scenario is illustrated in the following figure.

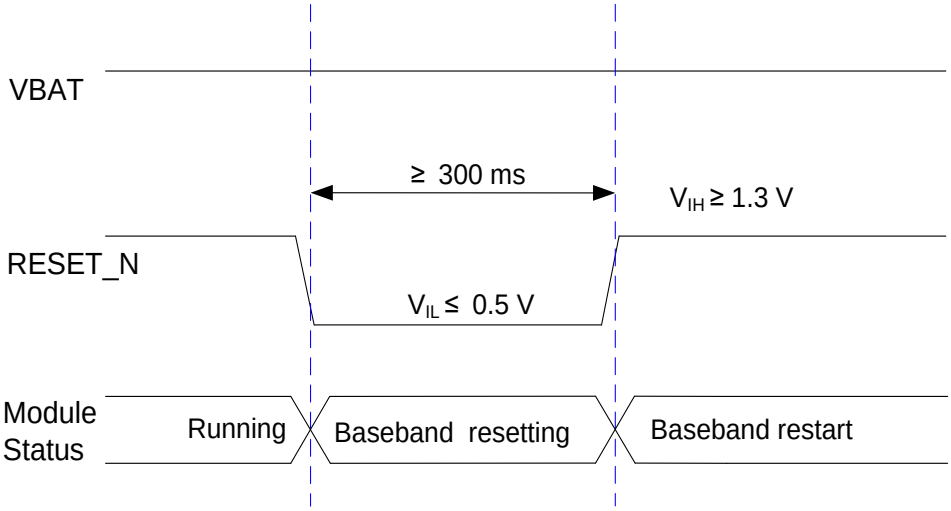


Figure 16: Reset Timing

NOTE

1. Ensure that the load capacitance does not exceed 10 nF on PWRKEY and RESET_N pins.
2. RESET_N only resets the internal baseband chip of the module and does not reset the power management chip.
3. Use RESET_N only when you fail to turn off the module with the **AT+QPOWD** and PWRKEY.

3.9. (U)SIM Interfaces

The module provides two (U)SIM interfaces, which meet ETSI and IMT-2000 requirements. Either 1.8 V or 3.0 V (U)SIM card is supported. The module supports Dual SIM Single Standby.

Table 12: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_DET	42	DI	(U)SIM1 card hot-swap detect	1.8 V power domain. If unused, keep it open.
USIM1_VDD	43	PO	(U)SIM1 card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM1_RST	44	DO	(U)SIM1 card reset	
USIM1_DATA	45	DIO	(U)SIM1 card data	
USIM1_CLK	46	DO	(U)SIM1 card clock	
USIM1_GND	47		Specified ground for (U)SIM1	Connect to main GND of PCB.
USIM2_DET	83	DI	(U)SIM2 card hot-swap detect	1.8 V power domain. If unused, keep it open.
USIM2_CLK	84	DO	(U)SIM2 card clock	
USIM2_RST	85	DO	(U)SIM2 card reset	
USIM2_DATA	86	DIO	(U)SIM2 card data	
USIM2_VDD	87	PO	(U)SIM2 card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.

The module supports (U)SIM card hot-swap via the USIM_DET pin, and both high and low level detection are supported. The function is disabled by default and can be configured via **AT+QSIMDET**. See ***document [2]*** for more details.

The following figure shows a reference design for (U)SIM card interface with an 8-pin (U)SIM card connector.

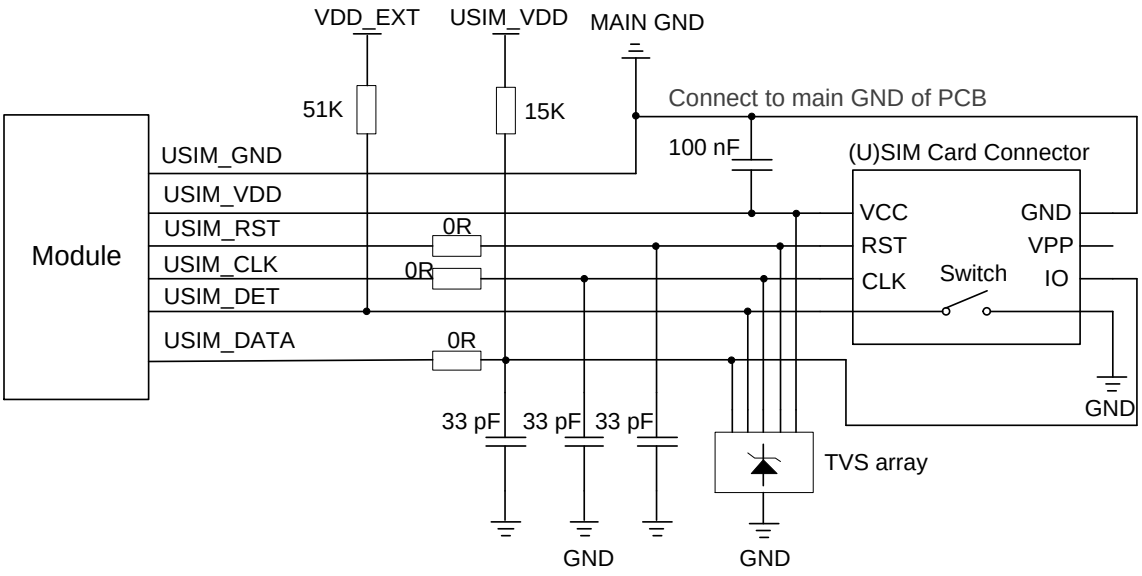


Figure 17: Reference Design of (U)SIM Interface with an 8-pin (U)SIM Card Connector

If the function of (U)SIM card hot-swap is not needed, please keep USIM_DET disconnected. A reference design for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

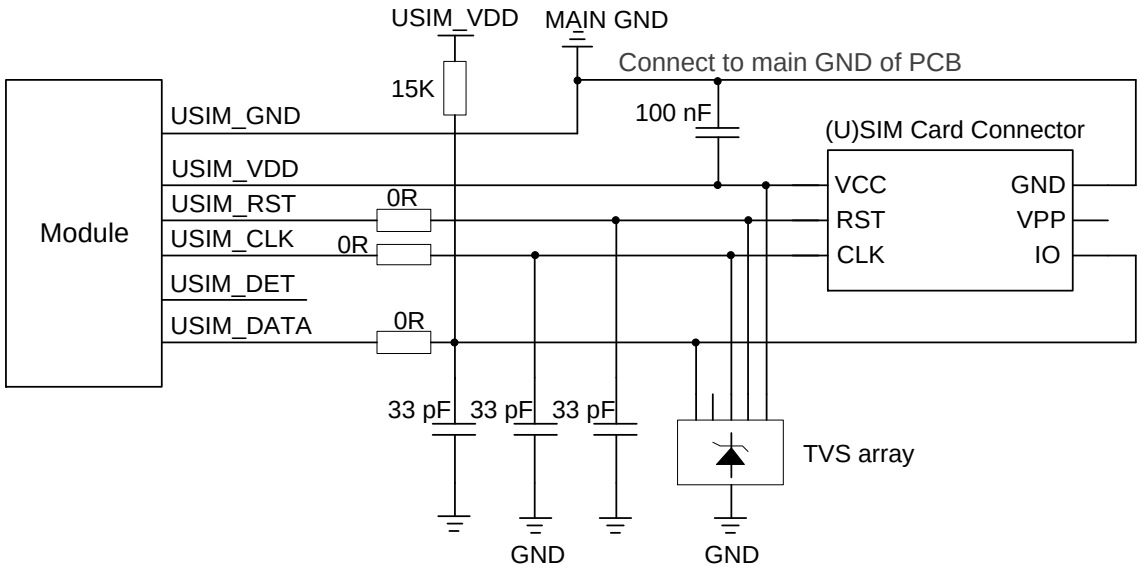


Figure 18: Reference Design of (U)SIM Interface with a 6-pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in your applications, please follow the criteria below in (U)SIM circuit design:

- Place the (U)SIM card connector as close to the module as possible. Keep the trace length as short as possible, at most 200 mm.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Make sure the ground between the module and the (U)SIM card connector is short and wide. Keep the trace width of ground and USIM_VDD not less than 0.5 mm to maintain the same electric potential. If the ground is complete on your PCB, USIM_GND can be connected to PCB ground directly.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- Make sure the bypass capacitor between USIM_VDD and GND less than 1 μF, and place it as close to the (U)SIM card connector as possible.
- To offer good ESD protection, it is recommended to add a TVS array whose parasitic capacitance should not be more than 15 pF. Add 0 Ω resistors in series between the module and the (U)SIM card to facilitate debugging. The 33 pF capacitors in parallel on USIM_DATA, USIM_CLK and USIM_RST lines are used for filtering interference of EGSM900. Note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA can improve anti-jamming capability of the (U)SIM card. If the (U)SIM card traces are too long, or the interference source is relatively close, it is recommended to add a pull-up resistor near the (U)SIM card connector.

3.10. USB Interface

The module provides one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports full-speed (12 Mbps) and high-speed (480 Mbps) modes. The USB interface can only serve in the slave mode and is used for AT command communication, data transmission, software debugging and firmware upgrade. The following table shows the pin definition of USB interface.

Table 13: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	8	AI	USB connection detect	Typical: 5.0 V If unused, keep it open.
USB_DP	9	AIO	USB differential data (+)	Requires differential impedance of 90 Ω. USB 2.0 compliant. If unused, keep them open.
USB_DM	10	AIO	USB differential data (-)	

For more details about the USB 2.0 specifications, please visit http://www.usb.org/home.

It is recommended to reserve test points for debugging and firmware upgrade in your designs. The following figure shows a reference design of USB interface.

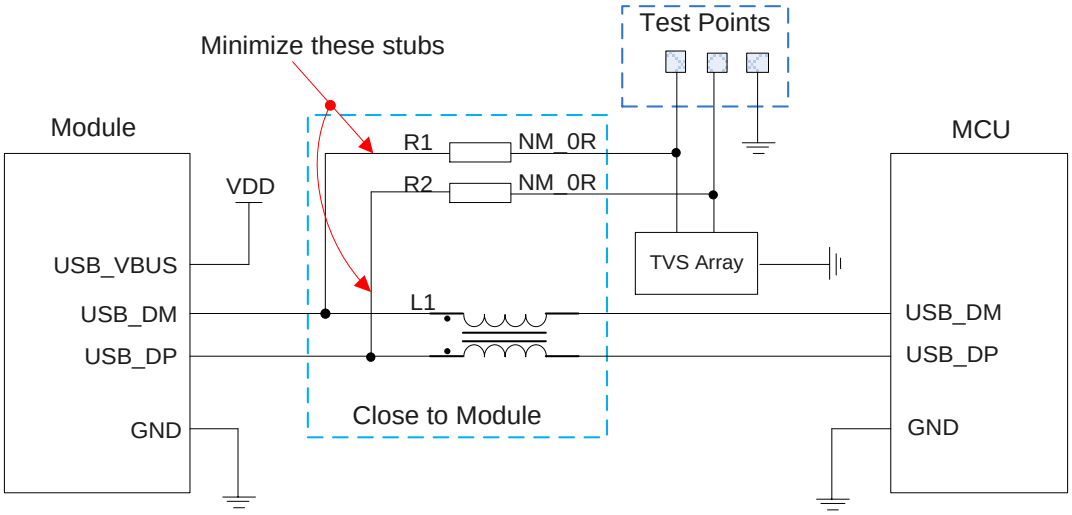


Figure 19: Reference Design of USB Application

A common mode choke L1 is recommended to be added in series between the module and MCU to suppress EMI spurious transmission. Meanwhile, the 0 Ω resistors (R1 and R2) should be added in series between the module and the test points to facilitate debugging, and the resistors are not mounted by default. To ensure the signal integrity of USB data lines, L1, R1 and R2 components must be placed close to the module, and resistors R1 and R2 should be placed close to each other. The extra stubs of trace must be as short as possible.

When designing the USB interface, you should follow the following principles to meet USB 2.0 specifications.

- Route the USB signal traces as a differential pair with ground surrounded. The impedance of USB differential trace is 90 Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. Route the USB differential traces of equal length in inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below.
- Pay attention to the selection of the ESD protection component on the USB data line. Its parasitic capacitance should not exceed 2 pF and should be placed as close as possible to the USB interface.

3.11. UART Interfaces

The module provides three UART interfaces: one main UART interface, one auxiliary UART interface* and one debug UART interface. Their features are described below.

- Main UART interface supports 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps, 921600 bps and 1 Mbps baud rates, and the default baud rate is 115200 bps. This interface is used for data transmission and AT command communication. Also, it supports RTS and CTS hardware flow control.
- Auxiliary UART* interface supports RTS and CTS hardware flow control.
- Debug UART interface supports 115200 bps baud rate. It is used for partial log output.

Table 14: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
MAIN_DTR	30	DI	Main UART data terminal ready	1.8 V power domain. If unused, keep them open.
MAIN_RXD	34	DI	Main UART receive	
MAIN_TXD	35	DO	Main UART transmit	
MAIN_CTS	36	DO	DTE clear to send signal from DCE	Connect to DTE's CTS. 1.8 V power domain. If unused, keep it open.
MAIN_RTS	37	DI	DTE request to send signal to DCE	Connect to DTE's RTS. 1.8 V power domain. If unused, keep it open.
MAIN_DCD	38	DO	Main UART data carrier detect	1.8 V power domain. If unused, keep them open.
MAIN_RI	39	DO	Main UART ring indication	

Table 15: Pin Definition of Auxiliary UART Interface

Pin Name	Pin No.	I/O	Description	Comment
AUX_RTS*	25	DI	DTE request to send signal to DCE	Connect to DTE's RTS. 1.8 V power domain. If unused, keep it open.
AUX_CTS*	26	DO	DTE clear to send signal from DCE	Connect to DTE's CTS. 1.8 V power domain. If unused, keep it open.

AUX_TXD*	27	DO	Auxiliary UART transmit	1.8 V power domain. If unused, keep them open.
AUX_RXD*	28	DI	Auxiliary UART receive	

Table 16: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_RXD	22	DI	Debug UART receive	1.8 V power domain. If unused, keep them open.
DBG_TXD	23	DO	Debug UART transmit	

The module provides a 1.8 V UART interface. Use a voltage-level translator if the application is equipped with a 3.3 V UART interface. A voltage-level translator TXS0108EPWR provided by Texas Instruments is recommended. The following figure shows a reference design.

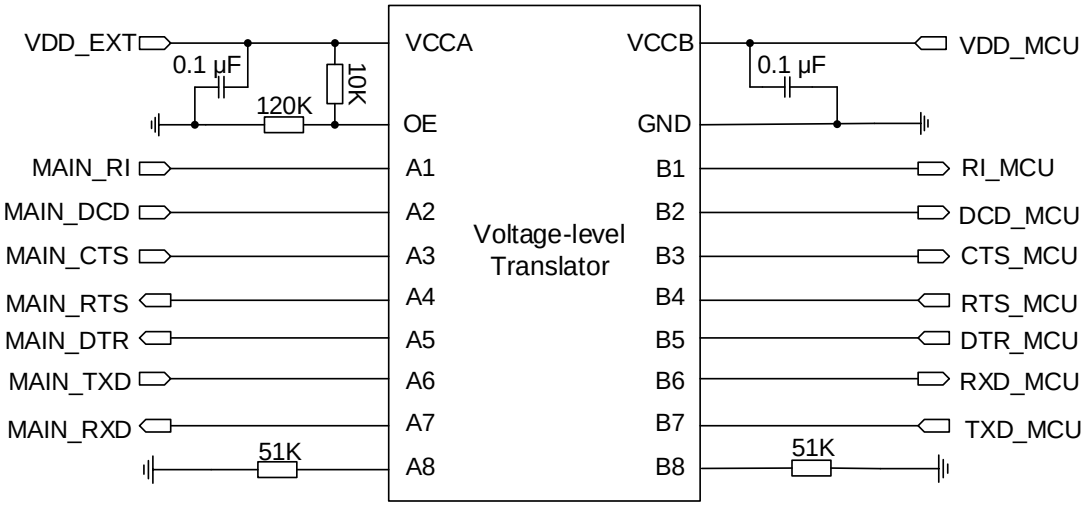


Figure 20: Reference Design with a Voltage-level Translator

Visit http://www.ti.com for more information.

Another example with transistor circuit is shown as below. For the design of circuits in dotted lines, see that shown in solid lines, but pay attention to the direction of connection.

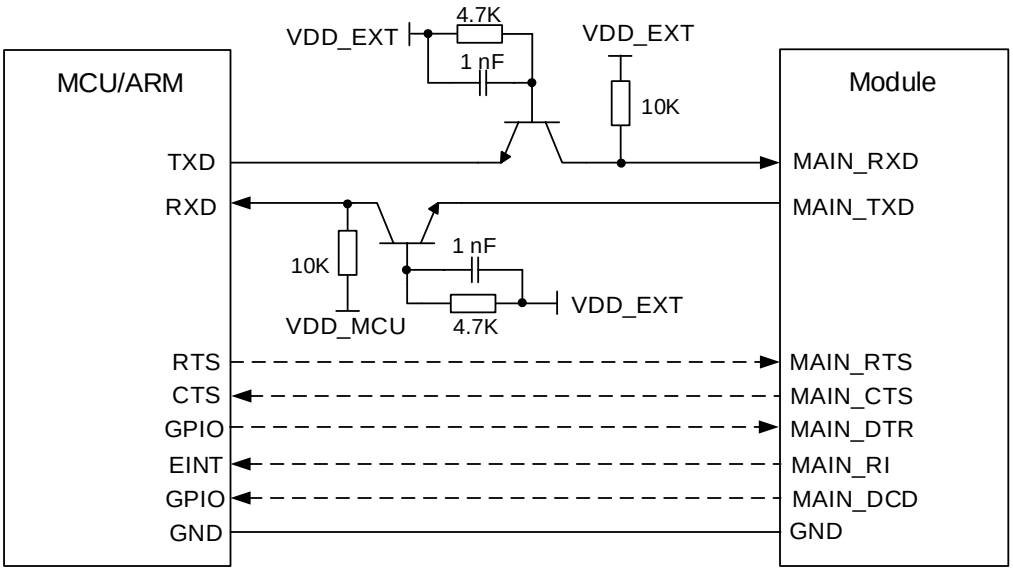


Figure 21: Reference Design with Transistor Circuit

NOTE

1. Transistor circuit solution is not suitable for applications with baud rates exceeding 460 kbps.
2. Note that the module CTS is connected to the host CTS, and the module RTS is connected to the host RTS.

3.12. Analog Audio Interfaces

The module provides one analog input channel and one analog output channel.

Table 17: Pin Definition of Audio Interfaces

Pin Name	Pin No.	I/O	Description	Comment
MICBIAS	120	PO	Bias voltage output for microphone	If unused, keep them open.
MIC_P	126	AI	Microphone analog input (+)	
MIC_N	119	AI	Microphone analog input (-)	
SPK_P	121	AO	Analog audio differential output (+)	The interface can drive

SPK_N	122	AO	Analog audio differential output (-)	32 Ω earpiece with power rate at 37 mW. It can also be used to drive external power amplifier devices if the output power rate cannot meet the demand. If unused, keep them open.

- AI channels are differential input channels, which can be applied for input of microphone (usually an electret microphone is used).
- AO channels are differential output channels, which can be applied for output of earpiece and loudspeaker.

You can use the **AT+QMIC** to adjust the input gain of the microphone, or **AT+CLVL** to adjust the volume gain output to the handset. The **AT+QSIDET** is used to set the side tone gain. For details, see ***document [3].***

3.12.1. Audio Interfaces Design Considerations

It is recommended to use the electret microphone with dual built-in capacitors (e.g. 10 pF and 33 pF) for filtering out RF interference, thus reducing TDD noise. The 33 pF capacitor is applied for filtering out RF interference when the module is transmitting at EGSM900. Without placing this capacitor, TDD noise could be heard. The 10 pF capacitor here is used for filtering out RF interference at DCS1800. Note that the resonant frequency point of a capacitor largely depends on the material and production technique. Therefore, you need to discuss with your capacitor vendors to choose the most suitable capacitor for filtering out high-frequency noises.

The severity degree of the RF interference in the voice channel during GSM transmitting largely depends on the application design. In some cases, EGSM900 TDD noise is more severe; while in other cases, DCS1800 TDD noise is more obvious. Therefore, a suitable capacitor can be selected based on the test results. The filter capacitor on the PCB should be placed as close as possible to the audio device or audio interface, and the wiring should be as short as possible. The filter capacitor should be passed before reaching other connection points.

To decrease radio or other signal interference, RF antennas should be placed away from audio interfaces and audio traces. Power traces cannot be parallel with and also should be far away from the audio traces.

The differential audio traces must be routed according to the differential signal layout rule.

3.12.2. Microphone Interface Design

The microphone channel reference design is shown in the following figure.

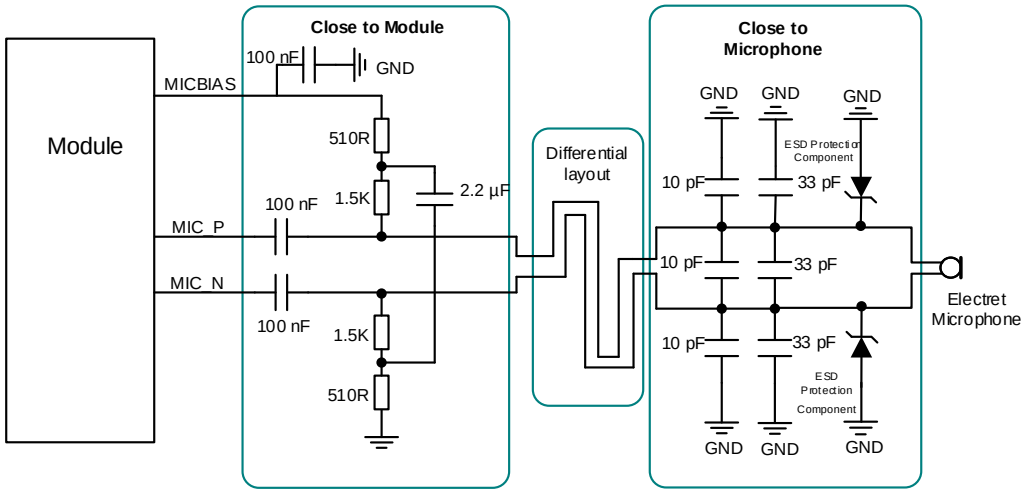


Figure 22: Reference Design for Microphone Interface

NOTE

MIC channel is sensitive to ESD, so it is not recommended to remove the ESD protection components used for protecting the MIC.

3.12.3. Earpiece and Loudspeaker Interface Design

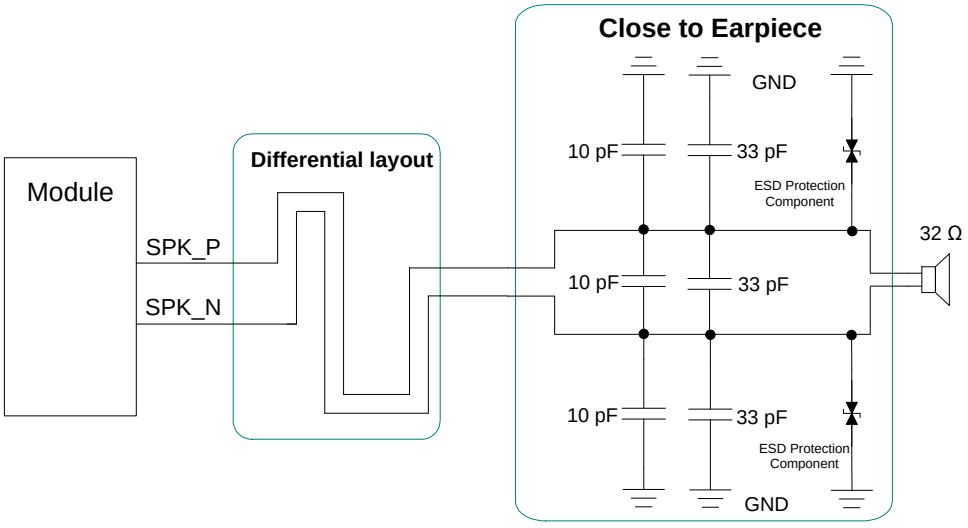


Figure 23: Reference Design for Earpiece Interface

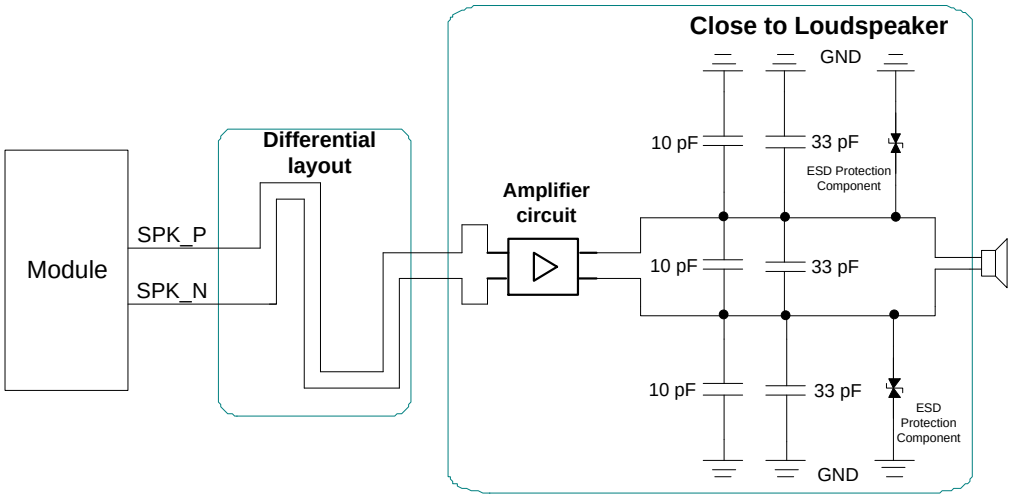


Figure 24: Reference Design of External Audio Amplifier Output

For differential input and output audio power amplifiers, please visit http://www.ti.com to obtain the required devices. There are also many audio power amplifiers with the same performance to choose from on the market.

3.13. PCM and I2C Interfaces

The module provides one Pulse Code Modulation (PCM) interface and one I2C interface.

Table 18: Pin Definition of PCM and I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM_CLK	4	DO	PCM clock	1.8 V power domain. If unused, keep them open.
PCM_SYNC	5	DO	PCM data frame sync	
PCM_DIN	6	DI	PCM data input	
PCM_DOUT	7	DO	PCM data output	
I2C_SCL	40	OD	I2C serial clock	An external 1.8 V pull-up resistor is required. If unused, keep it open.
I2C_SDA	41	OD	I2C serial data	

PCM interface supports short frame mode: module can only be used as master device.

The module supports 16-bit linear encoding format. The following figure is the short frame mode timing diagram (PCM_SYNC = 8 kHz, PCM_CLK = 2048 kHz).

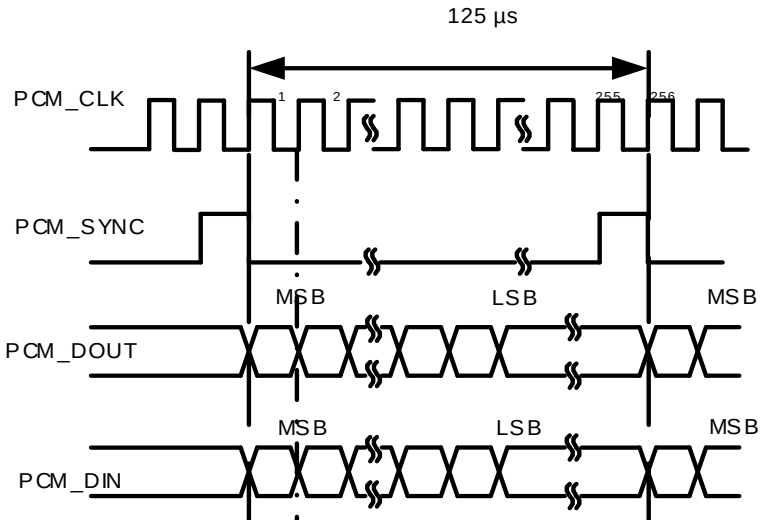


Figure 25: Timing of Short Frame Mode

In short frame mode, data is sampled on the falling edge of PCM_CLK, and sent on the rising edge. The falling edge of PCM_SYNC represents the high effective bit. In this mode, the PCM interface supports 256 kHz, 512 kHz, 1024 kHz, and 2048 kHz PCM_CLK at 8 kHz PCM_SYNC, and 4096 kHz PCM_CLK at 16 kHz PCM_SYNC.

The default configuration is short frame mode, PCM_CLK = 2048 kHz, PCM_SYNC =8 kHz.

The following figure shows a reference design of PCM interface with an external codec IC.

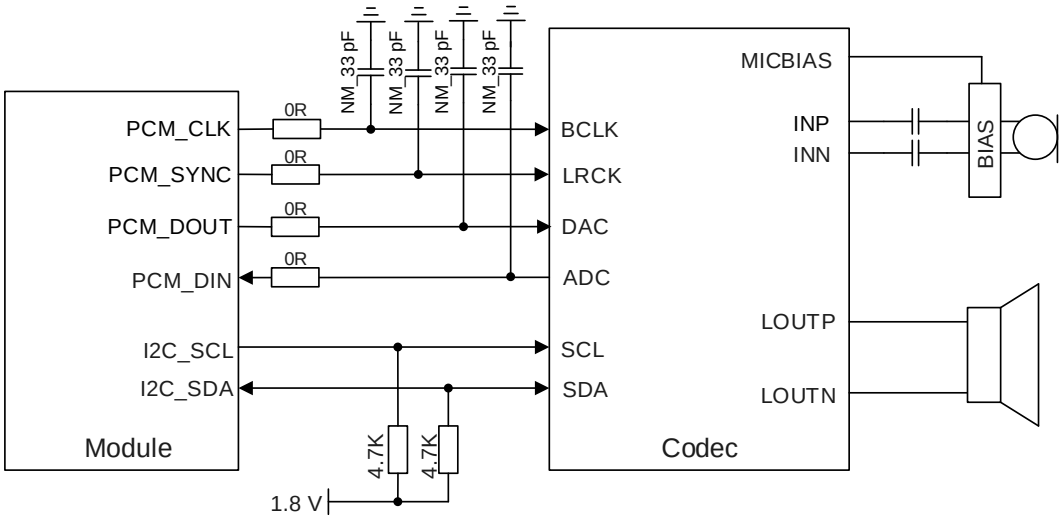


Figure 26: Reference Design of PCM and I2C Application with Audio Codec

NOTE

1. It is recommended to reserve an RC (R = 0 Ω, C = 33 pF) circuit on the PCM traces, especially for PCM_CLK.
2. The module can only be used as a master device in applications related to PCM and I2C interfaces.

3.14. Network Status Indication

The network indication pins can drive the network status indicators. The module provides a network status indication pin: NET_STATUS. The following tables describe pin definition and logic level changes in different network status.

Table 19: Pin Definition of Network Connection Status/Activity Indication

Pin Name	Pin No.	I/O	Description	Comment
NET_STATUS	21	DO	Indicate the module's network activity status	1.8 V power domain. If unused, keep it open.

Table 20: Working State of Network Activity Indicator

Pin Name	Logic Level Changes	Network Status
NET_STATUS	Flicker slowly (200 ms high/1800 ms low)	Network searching
	Flicker slowly (1800 ms high/200 ms low)	Idle
	Flicker quickly (125 ms high/125 ms low)	Data transmission is ongoing
	Always High (Always on)	Voice calling

A reference design is shown in the following figure.

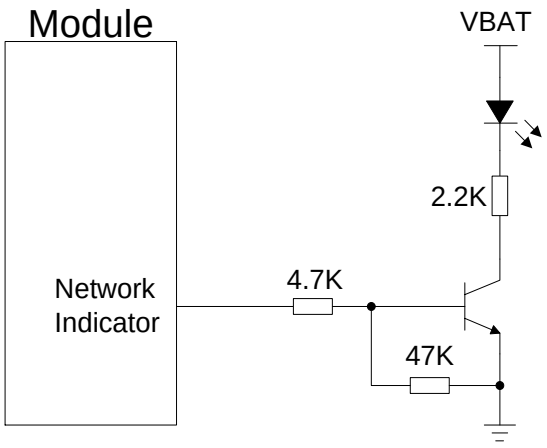


Figure 27: Reference Design of Network Status Indication

3.15. USB_BOOT

The module provides a USB_BOOT pin. Before the module is turned on, pull up USB_BOOT to 1.8 V, or short-circuit VDD_EXT and USB_BOOT, and the module will enter emergency download mode. In this mode, the module supports firmware upgrade over USB interface.

Table 21: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	75	DI	Force the module into emergency download mode	1.8 V power domain. Active high. It is recommended to reserve test points.

The following figure shows a reference design and timing sequence for entering emergency download mode of USB_BOOT interface.

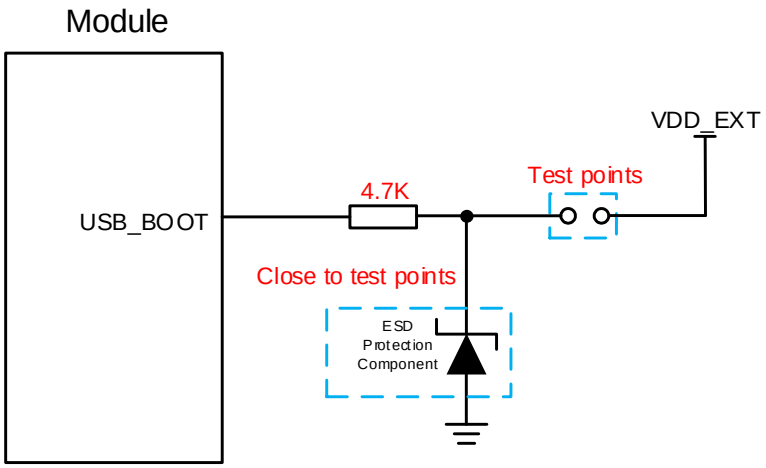


Figure 28: Reference Design of USB_BOOT Interface

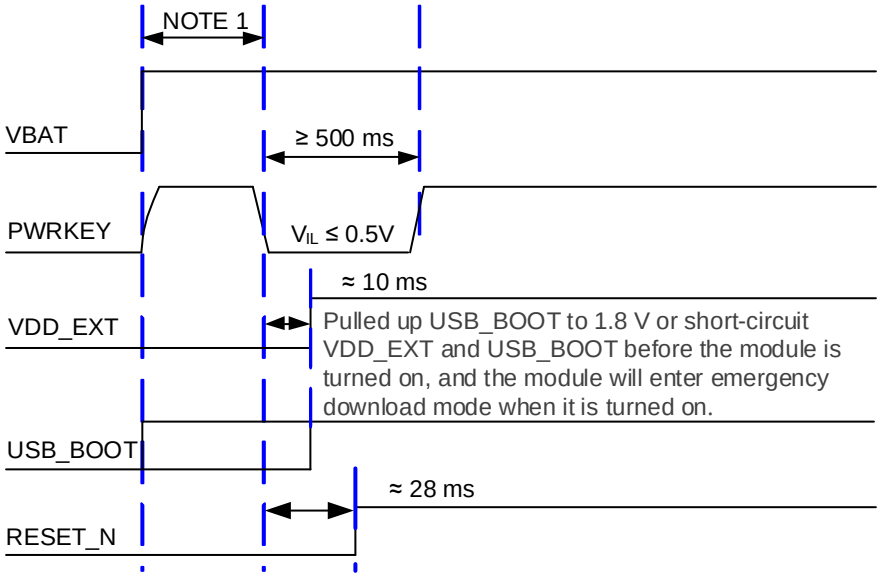


Figure 29: Timing Sequence for Entering Emergency Download Mode

NOTE

1. Make sure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time between powering up VBAT and pulling down PWRKEY pin is not less than 30 ms.
2. When using MCU to control module to enter the emergency download mode, please follow the above timing sequence. It is not recommended to pull up USB_BOOT to 1.8 V before powering up VBAT. Directly connect the test points as shown in ***Figure 28*** can manually force the module to enter download mode.

3.16. STATUS

The STATUS pin is an output for module's operation status indication. When the module is turned on normally, the STATUS will output high level.

Table 22: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	20	DO	Indicate the module's operation status	1.8 V power domain. If unused, keep it open.

The following figure shows a reference design of STATUS.

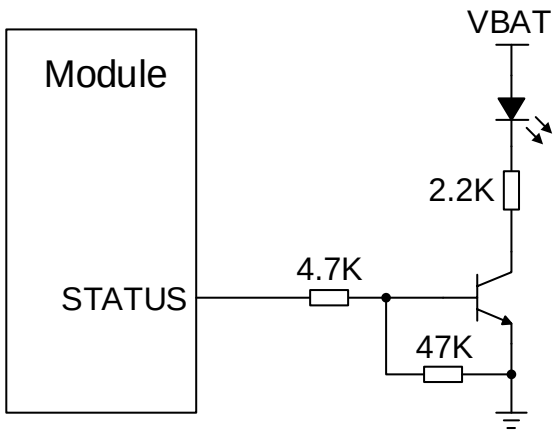


Figure 30: Reference Design of STATUS

3.17. ADC Interfaces

EG915N-EU provides two analog-to-digital conversion interfaces. **AT+QADC=0** can be used to read the voltage value on ADC0. **AT+QADC=1** can be used to read the voltage value on ADC1. For more details about these AT commands, see ***document [2].***

EG915N-LA does not support ADC function.

To improve the accuracy of ADC, surround the trace of ADC with ground.

Table 23: Pin Definition of EG915N-EU ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC1	2	AI	General-purpose ADC interface	If unused, keep them open.
ADC0	24	AI	General-purpose ADC interface	

Table 24: Characteristics of EG915N-EU ADC Interfaces

Parameter	Min.	Typ.	Max.	Unit
ADC0 voltage range	0	-	VBAT_BB	V
ADC1 voltage range	0	-	VBAT_BB	V
ADC resolution	-	-	12	bits

NOTE

1. When the module is not powered by VBAT, the ADC interface cannot be directly connected to any input voltage.
2. If the collected voltage is greater than 4.5 V, it is recommended to use a resistor divider circuit input for the ADC pin. When designing, reserve a 1 nF capacitor at both ends of the grounding divider resistor, which is not mounted by default.

3.18. MAIN_RI

Send **AT+QCFG="risignaltype","physical"** so that no matter on which port a URC is presented, the URC will trigger the behaviors of MAIN_RI pin.

NOTE

AT+QURCCFG allows you to set the main UART, USB AT port or USB modem port as the URC output port. The USB AT port is the URC output port by default.

You can configure MAIN_RI behaviors flexibly. The default behavior of the MAIN_RI is shown as below.

Table 25: Default Behaviors of the MAIN_RI

State	Response
Idle	MAIN_RI keeps at high level
URC	MAIN_RI outputs 120 ms low pulse when a new URC returns

The indication mode of MAIN_RI can be configured through multiple commands. For example, **AT+QCFG="urc/ri/ring"** can be used to configure the behavior of MAIN_RI during URC reporting. See ***document [2]*** for details.

4 GNSS

4.1. General Description

GNSS function is optional for the module. Only the module with built-in GNSS function integrates a multi-constellation GNSS receiver and supports GPS, GLONASS, Galileo, BDS, QZSS and SBAS positioning system. It also supports standard NMEA 0183 protocol and outputs NMEA sentences at 1 Hz data update rate via USB interface by default. The GNSS engine is turned off by default and can be turned on through AT commands. For more information, see ***document [4]***.

4.2. GNSS Performance

Table 26: GNSS Performance

Parameter	Description	Typ.	Unit
Sensitivity	Acquisition	-146	dBm
	Reacquisition	-160	dBm
	Tracking	-159	dBm
TTFF	Cold start @ open sky	28.01	s
	Warm start @ open sky	28.01	s
	Hot start @ open sky	4.05	s
Accuracy	CEP-50	1.72	m

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

4.3. GNSS Antenna Routing Guidelines

In your application design, the following design principles should be followed:

- The distance between the GNSS antenna and the main antenna should be as large as possible.
- Digital signals such as (U)SIM card, USB interface, camera module, SD card and display interface etc. should be far away from the antenna.
- Sensitive analog signals should be far away from GNSS signal paths, and ground holes should be added for isolation and protection.
- ANT_GNSS trace maintains 50 Ω characteristic impedance.

For the reference design of GNSS antenna interface and antenna precautions, see ***Chapter 5.2***.

5 RF Specifications

The module includes one main antenna interface. The module with built-in GNSS function also has one GNSS antenna interface. The impedance of antenna interface is 50 Ω.

5.1. Main Antenna Interface & Frequency Bands

5.1.1. Pin Definition

Table 27: Pin Definition of Main Antenna

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	60	AIO	Main antenna interface	50 Ω impedance.

5.1.2. Operating Frequency

Table 28: EG915N-EU Operating Frequency

3GPP Band	Transmit	Receive	Unit
EGSM900	880–915	925–960	MHz
DCS1800	1710–1785	1805–1880	MHz
LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B7	2500–2570	2620–2690	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-FDD B20	832–862	791–821	MHz

Table 29: EG915N-LA Operating Frequency

3GPP Band	Transmit	Receive	Unit
GSM850	824-849	869-894	MHz
EGSM900	880–915	925–960	MHz
DCS1800	1710–1785	1805–1880	MHz
PCS1900	1850-1910	1930-1990	MHz
LTE-FDD B2	1850-1910	1930-1990	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B4	1710-1755	2110-2155	MHz
LTE-FDD B5	824–849	869–894	MHz
LTE-FDD B7	2500–2570	2620–2690	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-FDD B28	703–748	758–803	MHz
LTE-FDD B66	1710–1780	2110–2180	MHz

5.1.3. Reference Design

A reference design of ANT_MAIN antenna is shown as below. A π-type matching circuit should be reserved for better RF performance. The capacitors are not mounted by default.

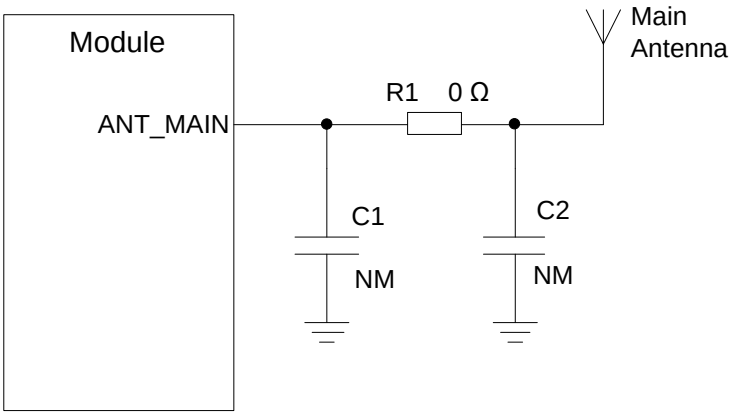


Figure 31: Reference Design for Main Antenna Interface

NOTE

Place the π-type matching components (R1, C1 and C2) as close to the antenna as possible.

5.1.4. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

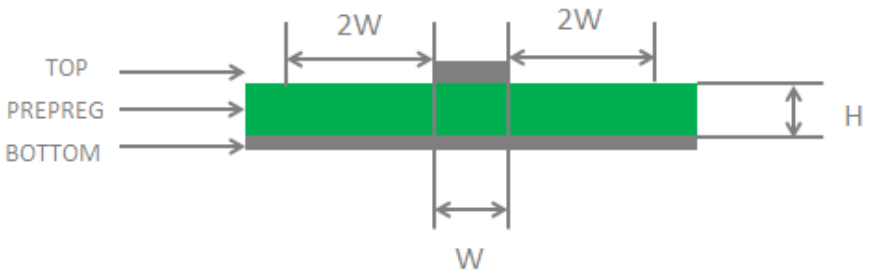


Figure 32: Microstrip Design on a 2-layer PCB

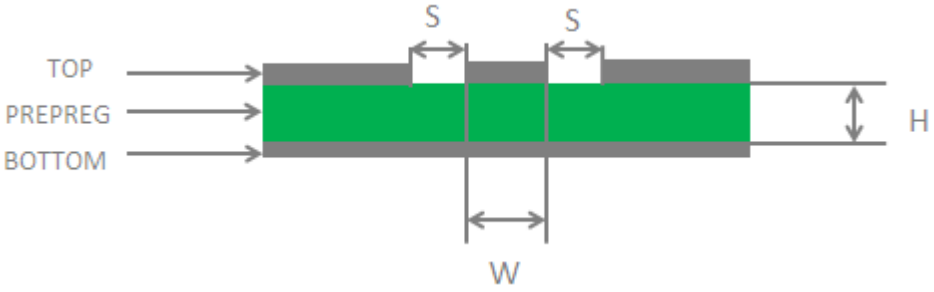


Figure 33: Coplanar Waveguide Design on a 2-layer PCB

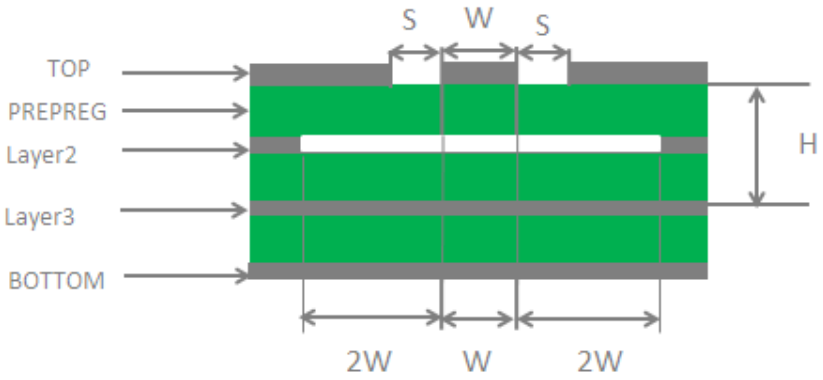


Figure 34: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

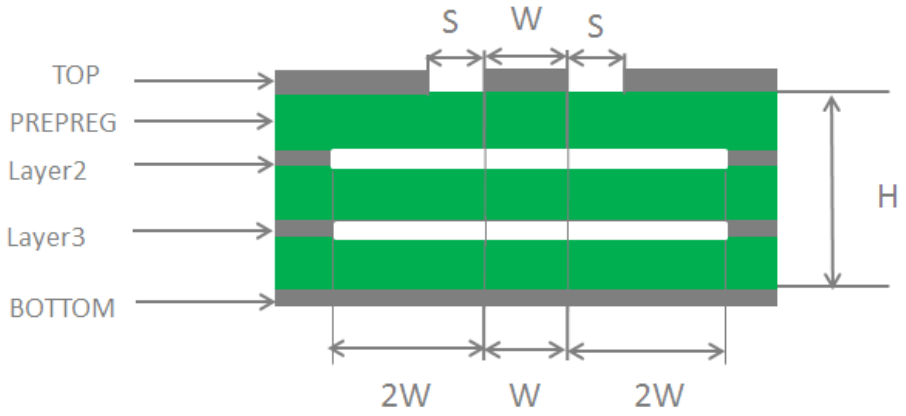


Figure 35: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be not less than twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [5]***.

5.2. GNSS Antenna Interface & Frequency Bands

The following tables list the pin definition and frequency characteristics of the GNSS antenna interface.

Table 30: GNSS Antenna Pin Definition

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	49	AI	GNSS antenna interface	50 Ω impedance. If unused, keep it open.

Table 31: GNSS Frequency

Type	Frequency	Unit
GPS	1575.42 ±1.023	MHz
GLONASS	1597.5–1605.8	MHz
Galileo	1575.42 ±2.046	MHz
BDS	1561.098 ±2.046	MHz
QZSS	1575.42	MHz
SBAS	1575.42	MHz

5.2.1. GNSS Antenna Reference Design

5.2.1.1. Reference Design for GNSS Active Antenna

GNSS active antenna connection reference design is shown in the figure below.

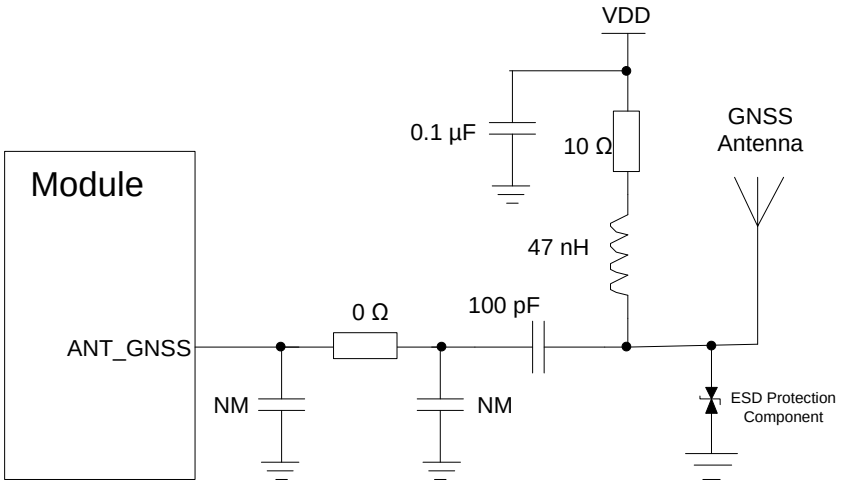


Figure 36: GNSS Active Antenna Reference Design

The power supply voltage range of the external active antenna is 2.8–4.3 V, and the typical value is 3.3 V.

NOTE

1. You can select an external LDO for power supply according to the active antenna requirements.
2. The junction capacitance of the antenna interface ESD protection component is recommended to be less than 0.05 pF.

5.2.1.2. Reference Design for GNSS Passive Antenna

GNSS passive antenna connection reference design is shown in the figure below.

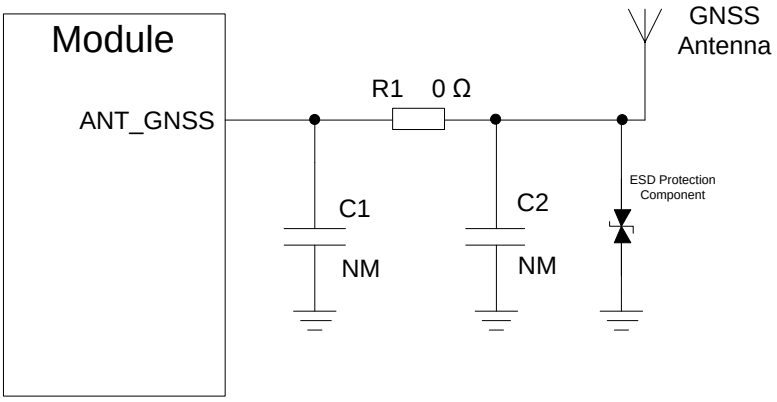


Figure 37: GNSS Passive Antenna Reference Design

C1, R1 and C2 form the matching circuit, which is recommended to be reserved for adjusting the antenna impedance. Among them, C1 and C2 are not mounted by default, and R1 is only mounted with 0 Ω resistor. The impedance of the RF trace should be controlled at about 50 Ω, and the trace should be as short as possible.

NOTE

1. If the module is designed with a passive antenna, then the VDD circuit is not needed.
2. The junction capacitance of the antenna interface ESD protection component is recommended to be less than 0.05 pF.

5.3. Antenna Design Requirements

5.3.1. Antenna Design Requirements

Table 32: Antenna Requirements

Type	Requirements
GSM/LTE	VSWR: ≤ 2 Efficiency: > 30 % Max input power: 50 W Input impedance: 50 Ω Cable insertion loss:

	● **< 1 dB:** LB (< 1 GHz) ● **< 1.5 dB:** MB (1–2.3 GHz) ● **< 2 dB:** HB (> 2.3 GHz)
GNSS	● Frequency range: L1:1559–1609 MHz ● Polarization: RHCP or linear ● VSWR: < 2 ● Passive antenna gain: > 0 dBi ● Active antenna noise factor: < 1.5 dB ● Active antenna gain: > -2 dBi ● Active antenna internal LNA gain: < 17 dB ● Active antenna total gain: < 17 dBi

5.3.2. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connector provided by Hirose.

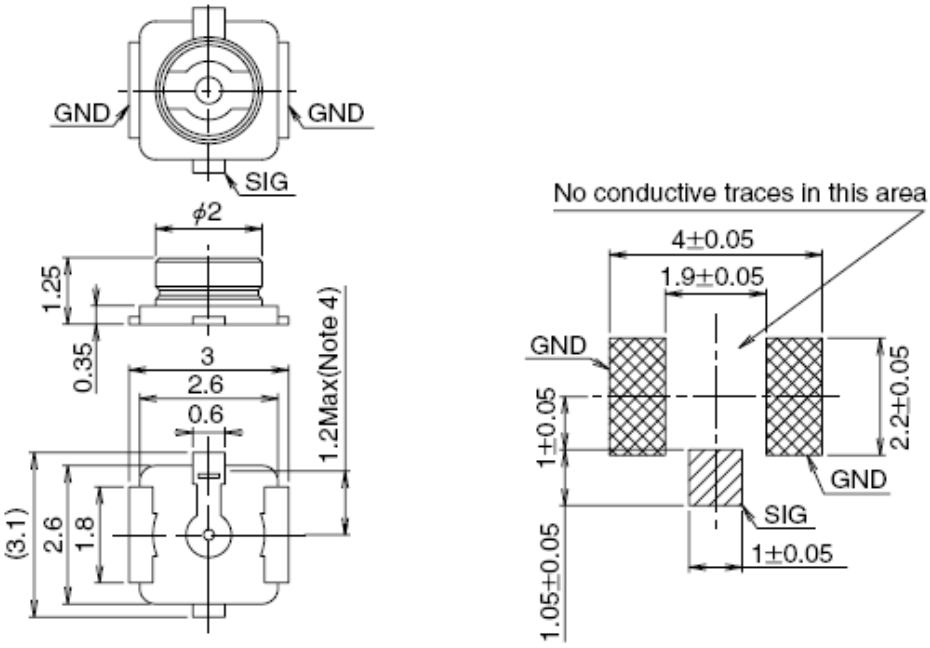


Figure 38: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series connectors listed in the following figure can be used to match the U.FL-R-SMT.

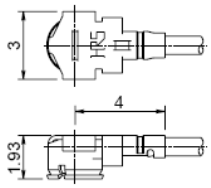
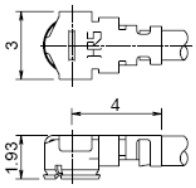
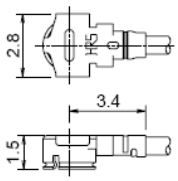
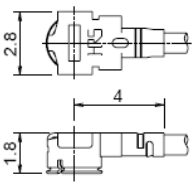
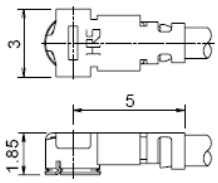
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 39: Specifications of Mated Plugs

The following figure describes the space factor of mated connector.

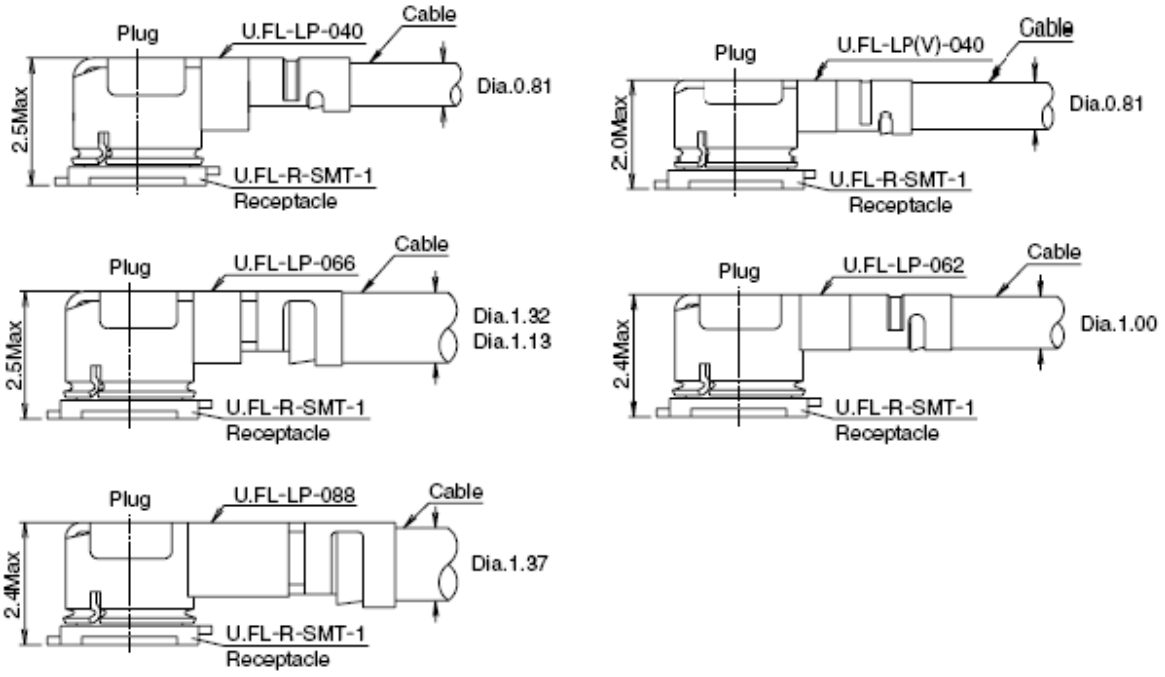


Figure 40: Space Factor of Mated Connectors (Unit: mm)

For more details, please visit http://hirose.com.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 33: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_BB	-0.3	6.0	V
VBAT_RF	-0.3	6.0	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	-	0.8	A
Peak Current of VBAT_RF	-	2.2	A
Voltage at Digital Pins	-0.3	2.3	V

6.2. Power Supply Ratings

Table 34: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must be kept between the minimum and maximum	3.4	3.8	4.5	V

		values.				
	Voltage drop during burst transmission	Maximum power control level on EGSM900.	-	-	400	mV
I_{VBAT}	Peak supply current (during transmission slot)	Maximum power control level on EGSM900.	-	2.0	2.5	A
USB_VBUS	USB connection detect		3.0	5.0	5.25	V

6.3. Digital I/O Characteristics

Table 35: 1.8 V Digital I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	Input high voltage	0.7 × VDDIO	VDDIO + 0.2	V
V_{IL}	Input low voltage	-0.3	0.3 × VDDIO	V
V_{OH}	Output high voltage	VDDIO - 0.2	-	V
V_{OL}	Output low voltage	-	0.2	V

Table 36: (U)SIM 1.8 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	1.62	1.98	V
V_{IH}	Input high voltage	0.7 × USIM_VDD	USIM_VDD	V
V_{IL}	Input low voltage	0	0.2 × USIM_VDD	V
V_{OH}	Output high voltage	0.7 × USIM_VDD	USIM_VDD	V
V_{OL}	Output low voltage	0	0.15 × USIM_VDD	V

Table 37: (U)SIM 3.0 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	2.7	3.3	V
V_{IH}	Input high voltage	0.7 × USIM_VDD	USIM_VDD	V
V_{IL}	Input low voltage	0	0.15 × USIM_VDD	V
V_{OH}	Output high voltage	0.7 × USIM_VDD	USIM_VDD	V
V_{OL}	Output low voltage	0	0.15 × USIM_VDD	V

6.4. Operating and Storage Temperatures

Table 38: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [4]	-35	+25	+75	ºC
Extended Operation Range [5]	-40	-	+85	ºC
Storage Temperature Range	-40	-	+90	ºC

6.5. Power Consumption

The power consumption of the module is shown in the table below.

Table 39: EG915N-EU Power Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	20	μA

[4] Within operating temperature range, the module is 3GPP compliant.
[5] Within extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission, emergency call, etc, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

Sleep state	**AT+CFUN=0** (USB disconnected)	0.81	mA
	EGSM900 @ DRX = 2 (USB disconnected)	1.84	mA
	EGSM900 @ DRX = 5 (USB disconnected)	1.35	mA
	EGSM900 @ DRX = 5 (USB suspend)	1.50	mA
	EGSM900 @ DRX = 9 (USB disconnected)	1.36	mA
	DCS1800 @ DRX = 2 (USB disconnected)	1.84	mA
	DCS1800 @ DRX = 5 (USB disconnected)	1.35	mA
	DCS1800 @ DRX = 5 (USB suspend)	1.50	mA
	DCS1800 @ DRX = 9 (USB disconnected)	1.20	mA
	LTE-FDD @ PF = 32 (USB disconnected)	1.80	mA
	LTE-FDD @ PF = 64 (USB disconnected)	1.37	mA
	LTE-FDD @ PF = 64 (USB suspend)	1.54	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.16	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.09	mA
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	19.26	mA
	EGSM900 @ DRX = 5 (USB connected)	28.41	mA
	LTE-FDD @ PF = 64 (USB disconnected)	19.36	mA
	LTE-FDD @ PF = 64 (USB connected)	28.49	mA
GPRS data transmission	EGSM900 4DL/1UL @ 32.15 dBm	229	mA
	EGSM900 3DL/2UL @ 31.99 dBm	385	mA
	EGSM900 2DL/3UL @ 31.08 dBm	496	mA
	EGSM900 1DL/4UL @ 28.86 dBm	518	mA
	DCS1800 4DL/1UL @ 29.03 dBm	162	mA
	DCS1800 3DL/2UL @ 28.90dBm	257	mA
	DCS1800 2DL/3UL @ 27.76 dBm	314	mA

	DCS1800 1DL/4UL @ 25.76 dBm	329	mA
EDGE data transmission	EGSM900 4DL/1UL @ 26.83 dBm	160	mA
	EGSM900 3DL/2UL @ 26.00 dBm	253	mA
	EGSM900 2DL/3UL @ 24.96 dBm	304	mA
	EGSM900 1DL/4UL @ 23.26 dBm	344	mA
	DCS1800 4DL/1UL @ 24.65 dBm	135	mA
	DCS1800 3DL/2UL @ 24.52 dBm	208	mA
	DCS1800 2DL/3UL @ 23.26 dBm	266	mA
	DCS1800 1DL/4UL @ 20.98 dBm	309	mA
LTE data transmission	LTE-FDD B1	491	mA
	LTE-FDD B3	496	mA
	LTE-FDD B7	510	mA
	LTE-FDD B8	456	mA
	LTE-FDD B20	427	mA
GSM voice call	EGSM900 PCL = 5 @ 32.14 dBm	227	mA
	EGSM900 PCL = 12 @ 19.60 dBm	101	mA
	EGSM900 PCL = 19 @ 5.54 dBm	79	mA
	DCS1800 PCL = 0 @ 29.02 dBm	158	mA
	DCS1800 PCL = 7 @ 15.99 dBm	81	mA
	DCS1800 PCL = 15 @ 0.24 dBm	64	mA

Table 40: EG915N-LA Power Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	26	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	0.86	mA

	EGSM900 @ DRX = 2 (USB disconnected)	1.89	mA
	EGSM900 @ DRX = 5 (USB disconnected)	1.41	mA
	EGSM900 @ DRX = 5 (USB suspend)	1.58	mA
	EGSM900 @ DRX = 9 (USB disconnected)	1.27	mA
	DCS1800 @ DRX = 2 (USB disconnected)	1.91	mA
	DCS1800 @ DRX = 5 (USB disconnected)	1.43	mA
	DCS1800 @ DRX = 5 (USB suspend)	1.59	mA
	DCS1800 @ DRX = 9 (USB disconnected)	1.29	mA
	LTE-FDD @ PF = 32 (USB disconnected)	1.68	mA
	LTE-FDD @ PF = 64 (USB disconnected)	1.29	mA
	LTE-FDD @ PF = 64 (USB suspend)	1.44	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.09	mA
	LTE-FDD @ PF = 256 (USB disconnected)	0.98	mA
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	15.94	mA
	EGSM900 @ DRX = 5 (USB connected)	27.94	mA
	LTE-FDD @ PF = 64 (USB disconnected)	15.62	mA
	LTE-FDD @ PF = 64 (USB connected)	27.61	mA
GPRS data transmission	GSM850 4DL/1UL @ 32.28 dBm	231	mA
	GSM850 3DL/2UL @ 32.15 dBm	414	mA
	GSM850 2DL/3UL @ 30.75 dBm	507	mA
	GSM850 1DL/4UL @ 28.56 dBm	532	mA
	EGSM900 4DL/1UL @ 32.46 dBm	236	mA
	EGSM900 3DL/2UL @ 32.34 dBm	427	mA
	EGSM900 2DL/3UL @ 31.05 dBm	527	mA
	EGSM900 1DL/4UL @ 28.74 dBm	545	mA

	DCS1800 4DL/1UL @ 29.72 dBm	176	mA
	DCS1800 3DL/2UL @ 29.57 dBm	308	mA
	DCS1800 2DL/3UL @ 27.99 dBm	364	mA
	DCS1800 1DL/4UL @ 26.06 dBm	394	mA
	PCS1900 4DL/1UL @ 29.75 dBm	165	mA
	PCS1900 3DL/2UL @ 29.62 dBm	290	mA
	PCS1900 2DL/3UL @ 28.24 dBm	352	mA
	PCS1900 1DL/4UL @ 26.26 dBm	379	mA
EDGE data transmission	GSM850 4DL/1UL @ 26.61 dBm	142	mA
	GSM850 3DL/2UL @ 26.38 dBm	238	mA
	GSM850 2DL/3UL @ 24.88 dBm	296	mA
	GSM850 1DL/4UL @ 22.34 dBm	319	mA
	EGSM900 4DL/1UL @ 27.14 dBm	146	mA
	EGSM900 3DL/2UL @ 26.61 dBm	254	mA
	EGSM900 2DL/3UL @ 25.39 dBm	311	mA
	EGSM900 1DL/4UL @ 23.04 dBm	341	mA
	DCS1800 4DL/1UL @ 25.97 dBm	136	mA
	DCS1800 3DL/2UL @ 25.91 dBm	235	mA
	DCS1800 2DL/3UL @ 24.74 dBm	298	mA
	DCS1800 1DL/4UL @ 22.17 dBm	340	mA
	PCS1900 4DL/1UL @ 26.15 dBm	132	mA
	PCS1900 3DL/2UL @ 26.08 dBm	229	mA
	PCS1900 2DL/3UL @ 24.67 dBm	288	mA
	PCS1900 1DL/4UL @ 22.18 dBm	329	mA
LTE data	LTE-FDD B2	520	mA

transmission	LTE-FDD B3	604	mA
	LTE-FDD B4	565	mA
	LTE-FDD B5	493	mA
	LTE-FDD B7	557	mA
	LTE-FDD B8	490	mA
	LTE-FDD B28	484	mA
	LTE-FDD B66	620	mA
GSM voice call	GSM850 PCL = 5 @ 32.24 dBm	240	mA
	GSM850 PCL = 12 @ 19.15 dBm	103	mA
	GSM850 PCL = 19 @ 5.10 dBm	71	Ma
	EGSM900 PCL = 5 @ 32.41 dBm	246	mA
	EGSM900 PCL = 12 @ 19.19 dBm	101	mA
	EGSM900 PCL = 19 @ 3.95 dBm	68	mA
	DCS1800 PCL = 0 @ 29.64 dBm	180	mA
	DCS1800 PCL = 7 @ 16.95 dBm	90	mA
	DCS1800 PCL = 15 @ 0.57 dBm	66	mA
	PCS1900 PCL = 0 @ 29.72 dBm	170	mA
	PCS1900 PCL = 7 @ 16.72 dBm	86	mA
	PCS1900 PCL = 15 @ 1.43 dBm	68	mA

6.6. Rx Sensitivity

The following tables show conducted RF receiving sensitivity of the module.

Table 41: EG915N-EU Conducted RF Receiving Sensitivity

Frequency Bands	Receiving Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
EGSM900	-109 dBm	-	-	-102 dBm
DCS1800	-104 dBm	-	-	-102 dBm
LTE-FDD B1 (10 MHz)	-98 dBm	-	-	-96.3 dBm
LTE-FDD B3 (10 MHz)	-98 dBm	-	-	-93.3 dBm
LTE-FDD B7 (10 MHz)	-97 dBm	-	-	-94.3 dBm
LTE-FDD B8 (10 MHz)	-98 dBm	-	-	-93.3 dBm
LTE-FDD B20 (10 MHz)	-98 dBm	-	-	-93.3 dBm

Table 42: EG915N-LA Conducted RF Receiving Sensitivity

Frequency Bands	Receiving Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
GSM850	-108 dBm	-	-	-102 dBm
EGSM900	-108 dBm	-	-	-102 dBm
DCS1800	-106 dBm	-	-	-102 dBm
PCS1900	-106 dBm	-	-	-102 dBm
LTE-FDD B2 (10 MHz)	-99 dBm	-	-	-94.3 dBm
LTE-FDD B3 (10 MHz)	-98 dBm	-	-	-93.3 dBm
LTE-FDD B4 (10 MHz)	-98.5 dBm	-	-	-9.3 dBm
LTE-FDD B5 (10 MHz)	-99.5 dBm	-	-	-94.3 dBm

LTE-FDD B7 (10 MHz)	-97 dBm	-	-	-94.3 dBm
LTE-FDD B8 (10 MHz)	-99 dBm	-	-	-93.3 dBm
LTE-FDD B28 (10 MHz)	-99 dBm	-	-	-94.8 dBm
LTE-FDD B66 (10 MHz)	-99 dBm	-	-	-96.5 dBm

6.7. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

The following table shows the module electrostatics discharge characteristics.

Table 43: Electrostatics Discharge Characteristics (25 ºC, 45 % Relative Humidity)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
All Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

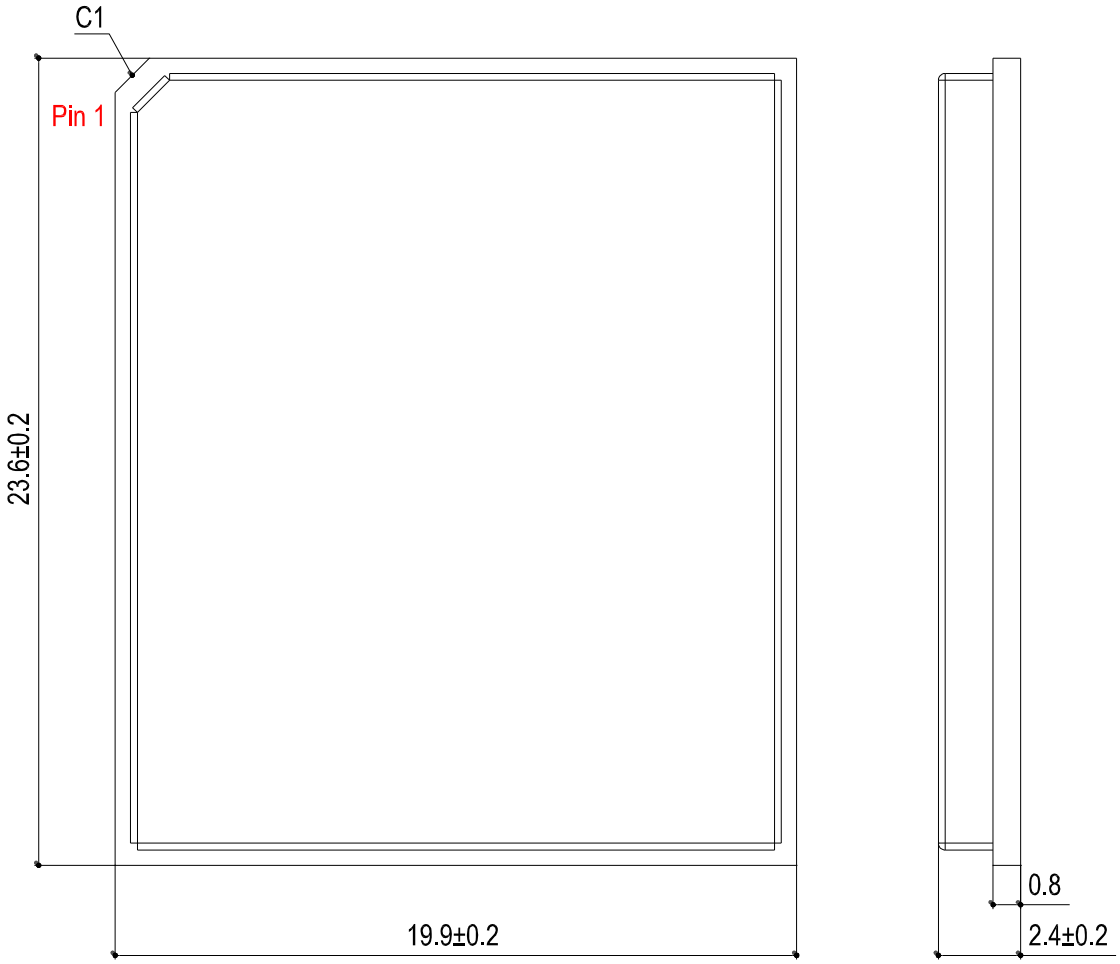


Figure 41: Top and Side Dimensions

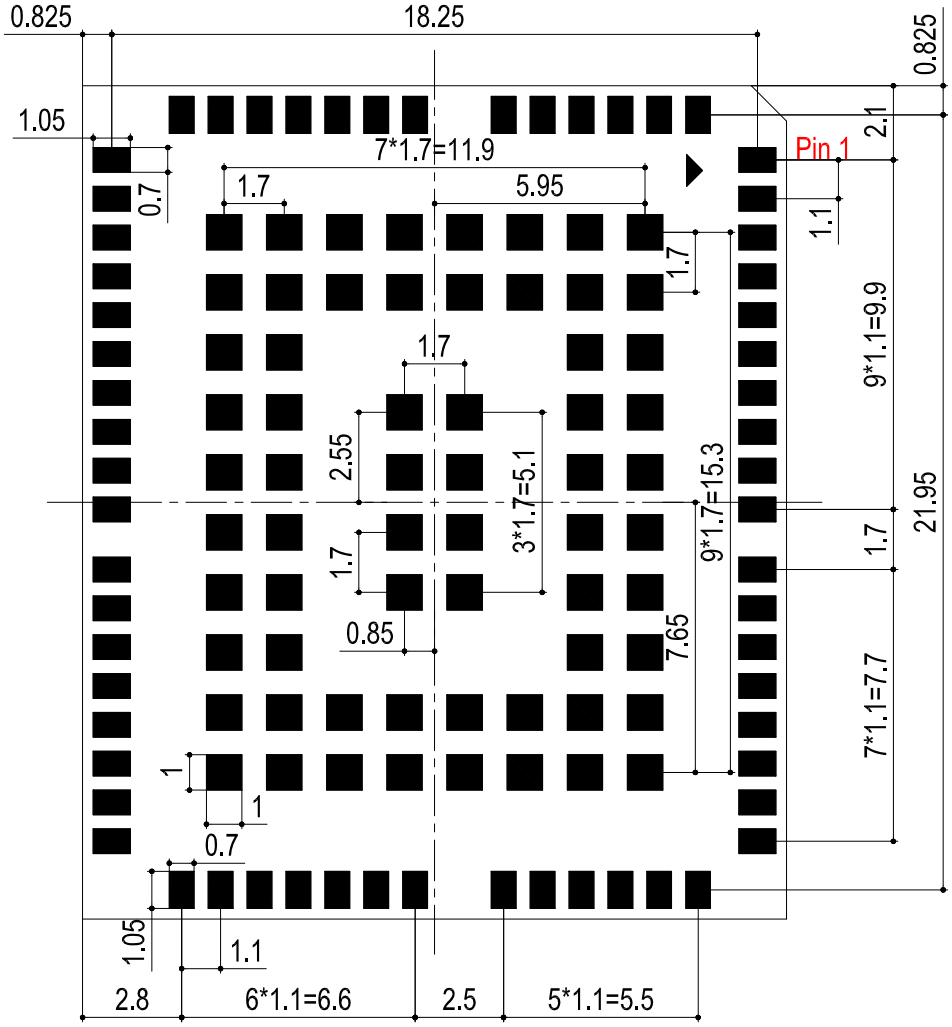


Figure 42: Bottom Dimensions (Bottom View)

NOTE

The package warpage level of the module conforms to *JEITA ED-7306* standard.

7.2. Recommended Footprint

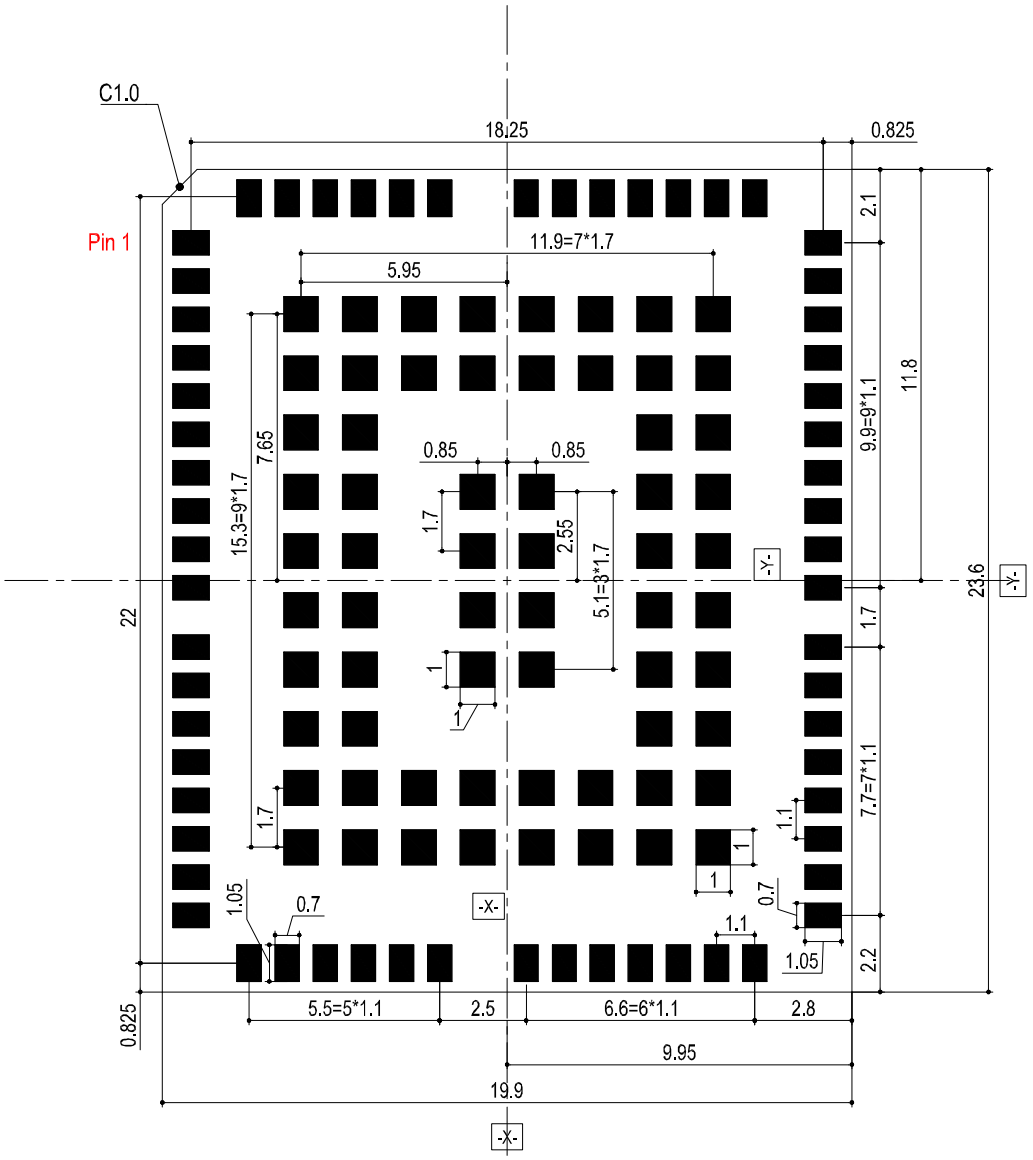


Figure 43: Recommended Footprint (Top View)

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Tx Power

The following tables show the RF output power of the module.

Table 44: EG915N-EU RF Output Power

Frequency Bands	Max. RF Output Power	Min. RF Output Power
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
EGSM900 (8-PSK)	27 dBm ±3 dB	5 dBm ±5 dB
DCS1800 (8-PSK)	26 dBm ±3 dB	0 dBm ±5 dB
LTE-FDD B1/B3/B7/B8/B20	23 dBm ±2 dB	< -39 dBm

Table 45: EG915N-LA RF Output Power

Frequency Bands	Max. RF Output Power	Min. RF Output Power
GSM850	33 dBm ±2 dB	5 dBm ±5 dB
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
PCS1800	30 dBm ±2 dB	0 dBm ±5 dB
GSM850 (8-PSK)	27 dBm ±3 dB	5 dBm ±5 dB
EGSM900 (8-PSK)	27 dBm ±3 dB	5 dBm ±5 dB
DCS1800 (8-PSK)	26 dBm ±3 dB	0 dBm ±5 dB
PCS1900 (8-PSK)	26 dBm ±3 dB	0 dBm ±5 dB
LTE-FDD B2/B3/B4/B5/B7/B8/B28/B66	23 dBm ±2 dB	< -39 dBm

NOTE

In GPRS 4 slots Tx mode, the maximum output power is reduced by 2.5 dB. The design conforms to the GSM specification as described in ***Chapter 13.16*** of *3GPP TS 51.010-1*.

7.4. Top and Bottom Views

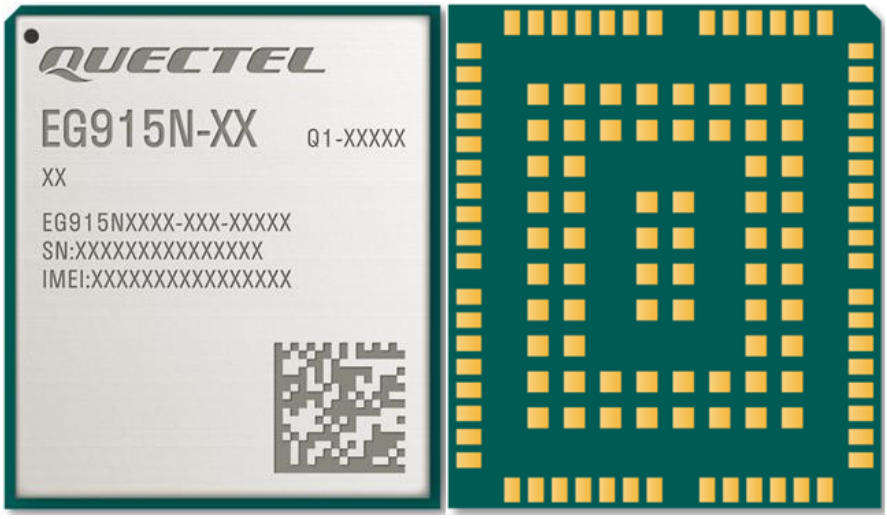


Figure 44: Top View and Bottom View of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. The storage life (in vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [6] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g. a drying cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement above occurs;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a drying cabinet.

[6] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not remove the packages of tremendous modules if they are not ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.15 mm. For more details, see ***document [6].***

The peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

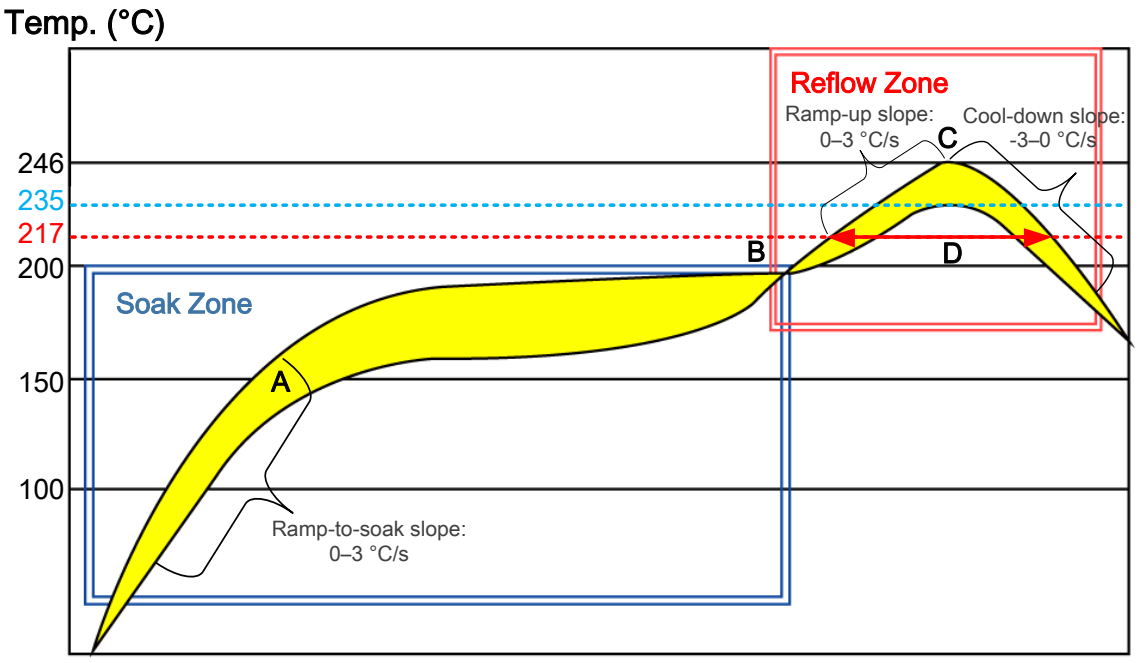


Figure 45: Recommended Reflow Soldering Thermal Profile

Table 46: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217°C)	40–70 s
Max temperature	235–246 °C
Cool-down slope	-3–0 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirement.
2. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
3. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6. Due to the complexity of the SMT process, please contact Quectel Technical Supports in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [6]***.

8.3. Packaging Specifications

This chapter describes only the key parameters and process of packaging. All figures below are for reference only. The appearance and structure of the packaging materials are subject to the actual delivery.

The module adopts carrier tape packaging and details are as follow:

8.3.1. Carrier Tape

Dimension details are as follow:

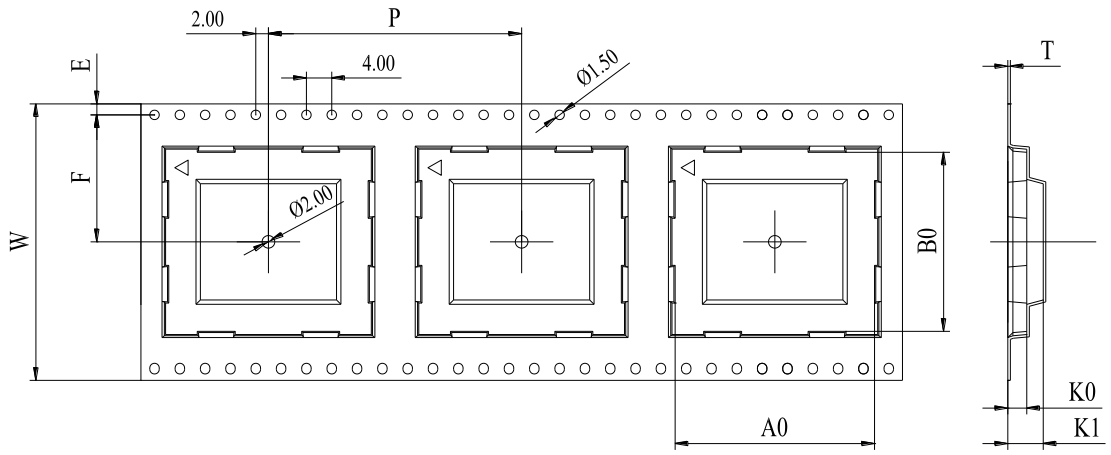


Figure 46: Carrier Tape Dimension Drawing

Table 47: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	32	0.35	20.2	24	3.15	6.65	20.2	1.75

8.3.2. Plastic Reel

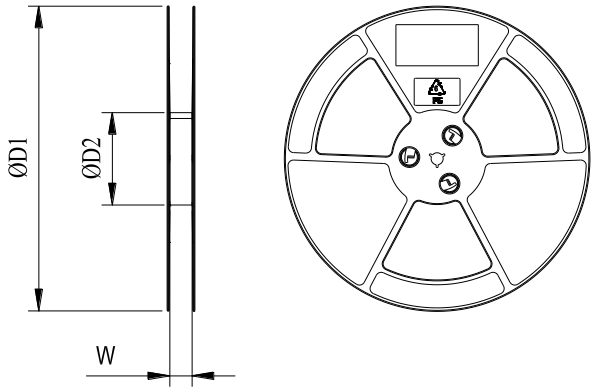
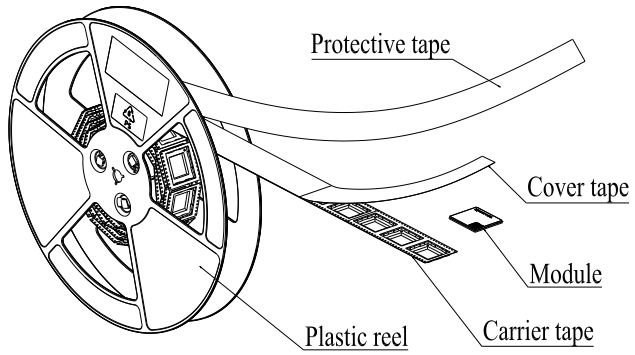


Figure 47: Plastic Reel Dimension Drawing

Table 48: Plastic Reel Dimension Table (Unit: mm)

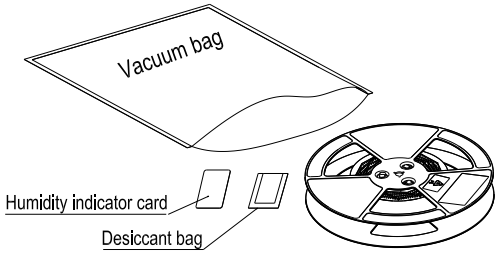
øD1	øD2	W
330	100	44.5

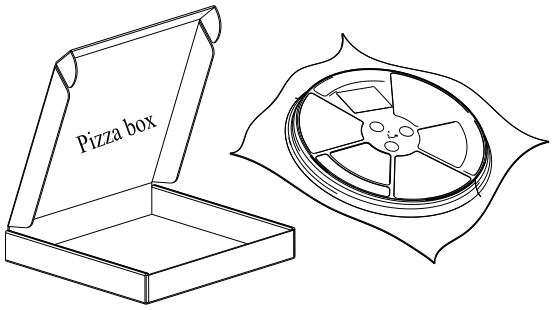
8.3.3. Packaging Process



Place the module into the carrier tape and use the cover tape to cover them; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. One plastic reel can load 250 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, then vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Put 4 pizza boxes into 1 carton and seal it. One carton can pack 1000 modules.

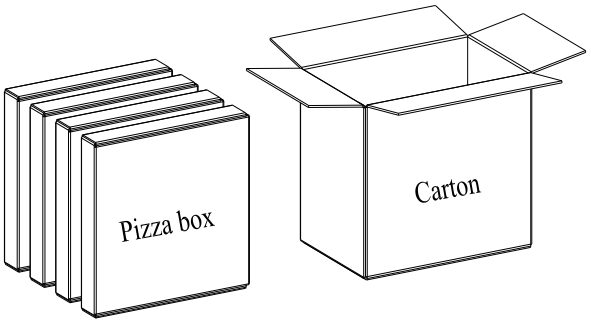


Figure 48: Packaging Process

9 Appendix References

Table 49: Related Documents

Document Name
[1] Quectel_UMTS&LTE_EVB_User_Guide
[2] Quectel_EC200x&EG912Y&EG915N_Series_AT_Commands_Manual
[3] Quectel_EC200x&EG912Y&EG915N_Series_Audio_Application_Note
[4] Quectel_EC200N-CN&EC800M-CN&EG915N_Series_GNSS_Application_Note
[5] Quectel_RF_Layout_Application_Note
[6] Quectel_Module_SMT_Application_Note

Table 50: Terms and Abbreviations

Abbreviation	Description
3GPP	3rd Generation Partnership Project
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-rate
BB	Baseband
BDS	BeiDou Navigation Satellite System
bps	Bits Per Second
CEP	Circular Error Probable
CHAP	Challenge Handshake Authentication Protocol
CMUX	Connection MUX

CS	Coding Scheme
CTS	Clear To Send
DCE	Data Communications Equipment
DCS	Data Coding Scheme
DFOTA	Delta Firmware Upgrade Over-The-Air
DL	Downlink
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EDGE	Enhanced Data Rates for GSM Evolution
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standards Institute
EVB	Evaluation Board
FDD	Frequency Division Duplex
FILE	File Protocol
FR	Full Rate
FTP	File Transfer Protocol
FTPS	FTP over SSL
Galileo	Galileo Satellite Navigation System (EU)
GLONASS	Global Navigation Satellite System (Russia)
GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System

GPIO	General-Purpose Input/Output
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile Communications
HR	Half Rate
HTTP	Hyper Text Transfer Protocol
HTTPS	Hyper Text Transfer Protocol over Secure Socket Layer
IMT-2000	International Mobile Telecommunications 2000
IOmax	Maximum Output Load Current
I2C	Inter-Integrated Circuit
LDO	Low Dropout Regulator
LED	Light Emitting Diode
LGA	Land Grid Array
LNA	Low-Noise Amplifier
LTE	Long Term Evolution
M2M	Machine to Machine
Mbps	Megabits per second
MCS	Modulation and Coding Scheme
ME	Mobile Equipment
MIC	Microphone
MLCC	Multi-layer Ceramic Capacitor
MMS	Multimedia Messaging Service
MO	Mobile Origination
MQTT	Message Queuing Telemetry Transport
MSL	Moisture Sensitivity Level

MT	Mobile Terminating
NITZ	Network Identity and Time Zone
NMEA	(National Marine Electronics Association)0183 Interface Standard
NTP	Network Time Protocol
PA	Power Amplifier
PAM	Power Amplifier Module
PAP	Password Authentication Protocol
PC	Personal Computer
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDA	Personal Digital Assistant
PDU	Protocol Data Unit
PF	Paging Frame
PING	Packet Internet Groper
PMIC	Power Management IC
POS	Point of Sale
PPP	Point-to-Point Protocol
PPS	Pulse Per Second
PSK	Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RAM	Random Access Memory
RHCP	Right Hand Circular Polarization
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
RTS	Request to Send

SAW	Surface Acoustic Wave
SBAS	Satellite-Based Augmentation System
SIM	Subscriber Identity Module
SIMO	Single Input Multiple Output
SMD	Surface Mount Device
SMS	Short Message Service
SMT	Surface Mount Technology
SMTP	Simple Mail Transfer Protocol
SMTPS	Simple Mail Transfer Protocol Secure
SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
TDD	Time Division Duplexing
TTFF	Time to First Fix
TVS	Transient Voltage Suppressor
UART	Universal Asynchronous Receiver &Transmitter
UDP	User Datagram Protocol
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
VBAT	Voltage at Battery (Pin)
V_{IH}	High-level Input Voltage
V_{IL}	Low-level Input Voltage
Vmax	Maximum Voltage

Vmin	Minimum Voltage
Vnom	Nominal Voltage
V_{OH}	High-level Output Voltage
V_{OL}	Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio